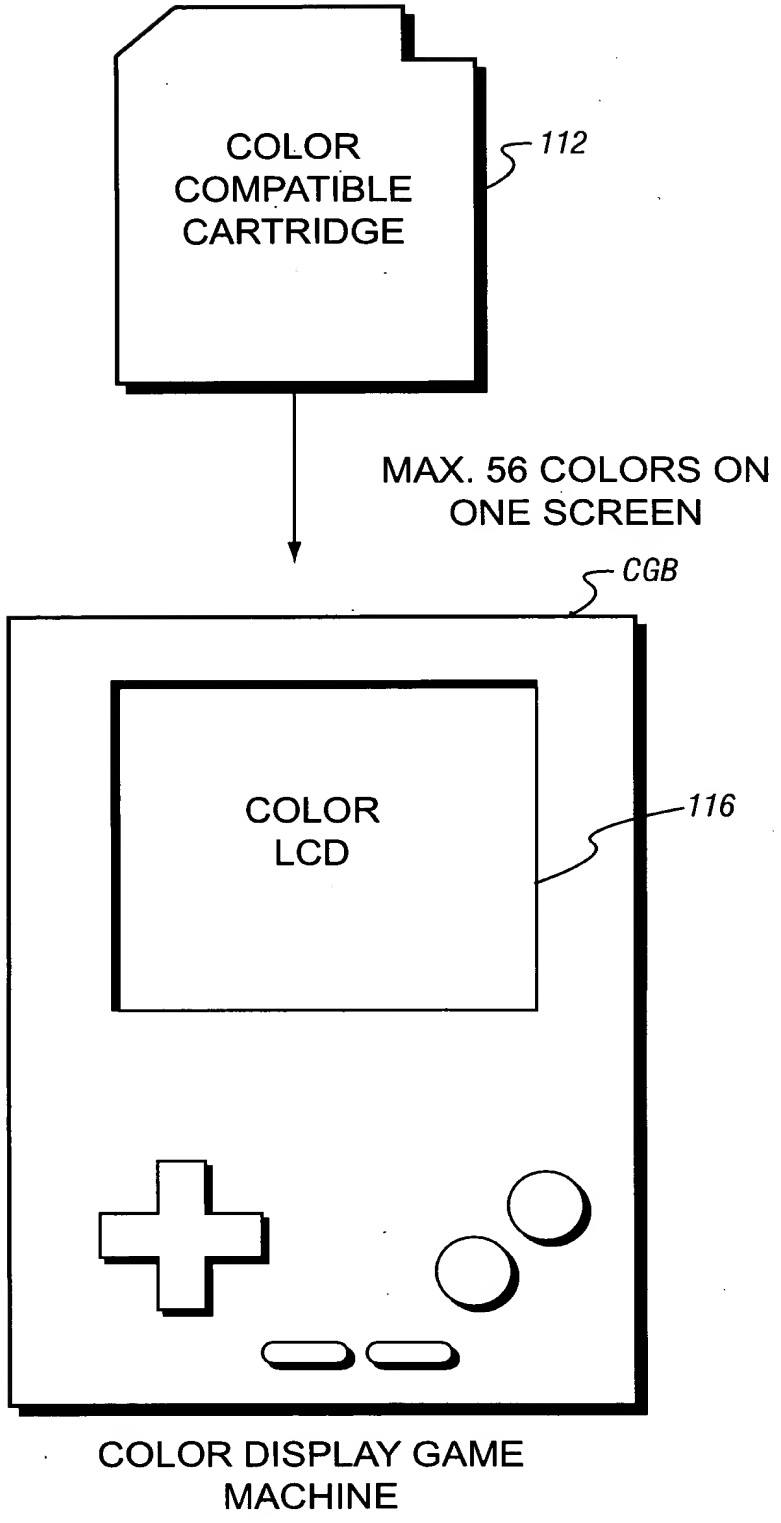

COLOR
COMPATIBLE
CARTRIDGE
112
MAX. 56 COLORS ON
ONE SCREEN
CGB
COLOR
LCD
116
COLOR DISPLAY GAME
MACHINE

Fig. 1A

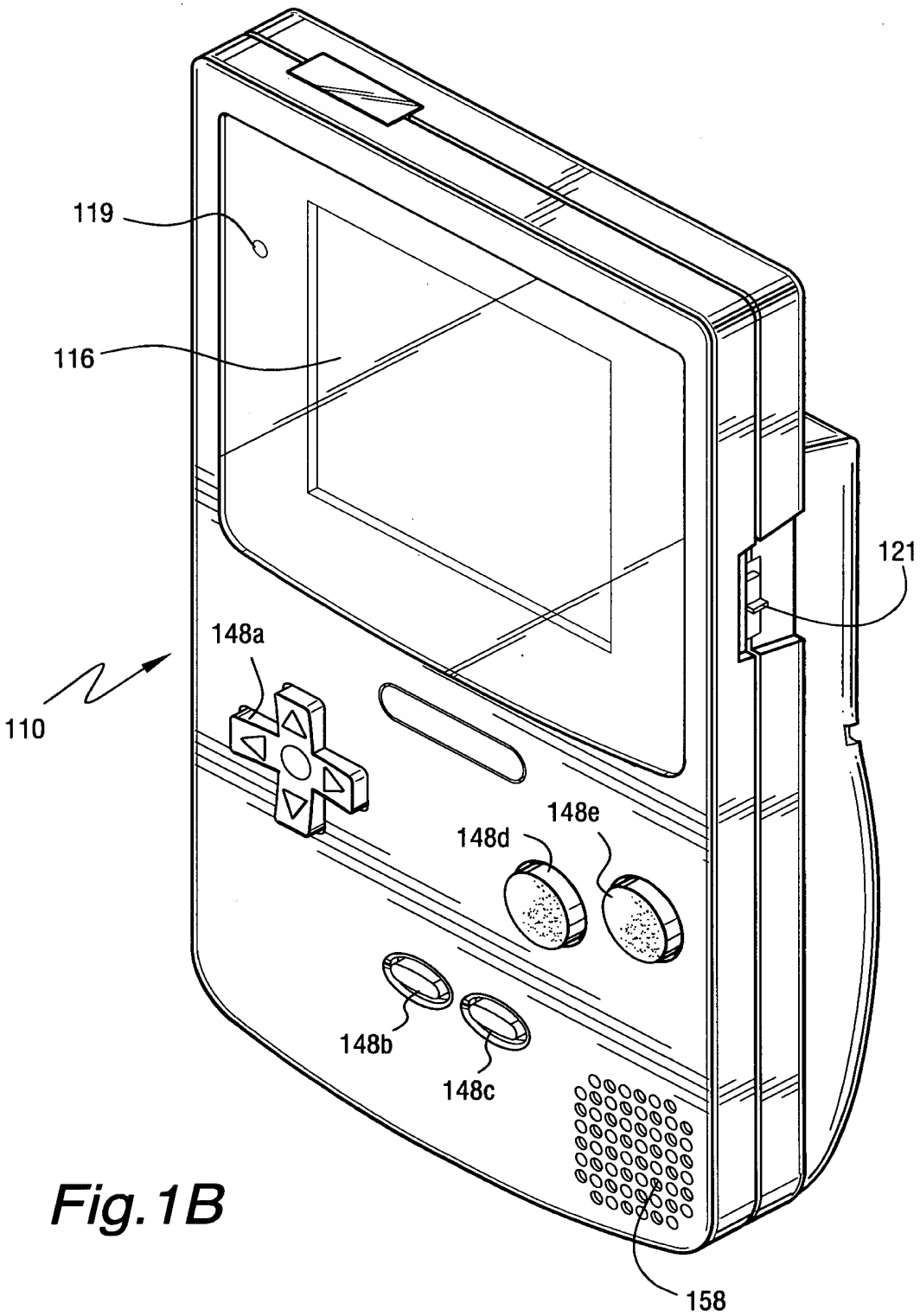


Fig.1B

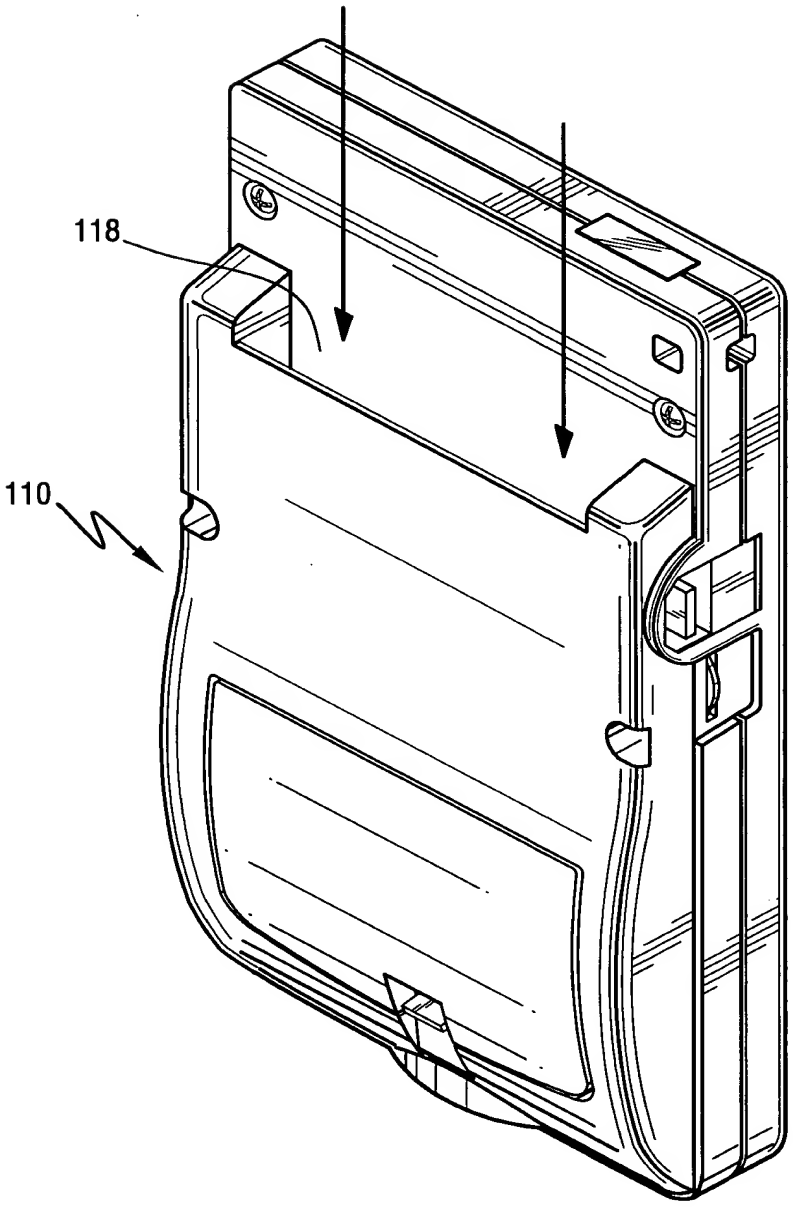
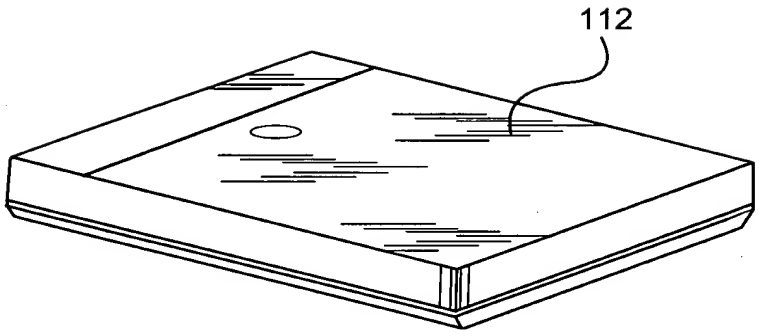


Fig.1C

Fig. 2

(Prior Art)



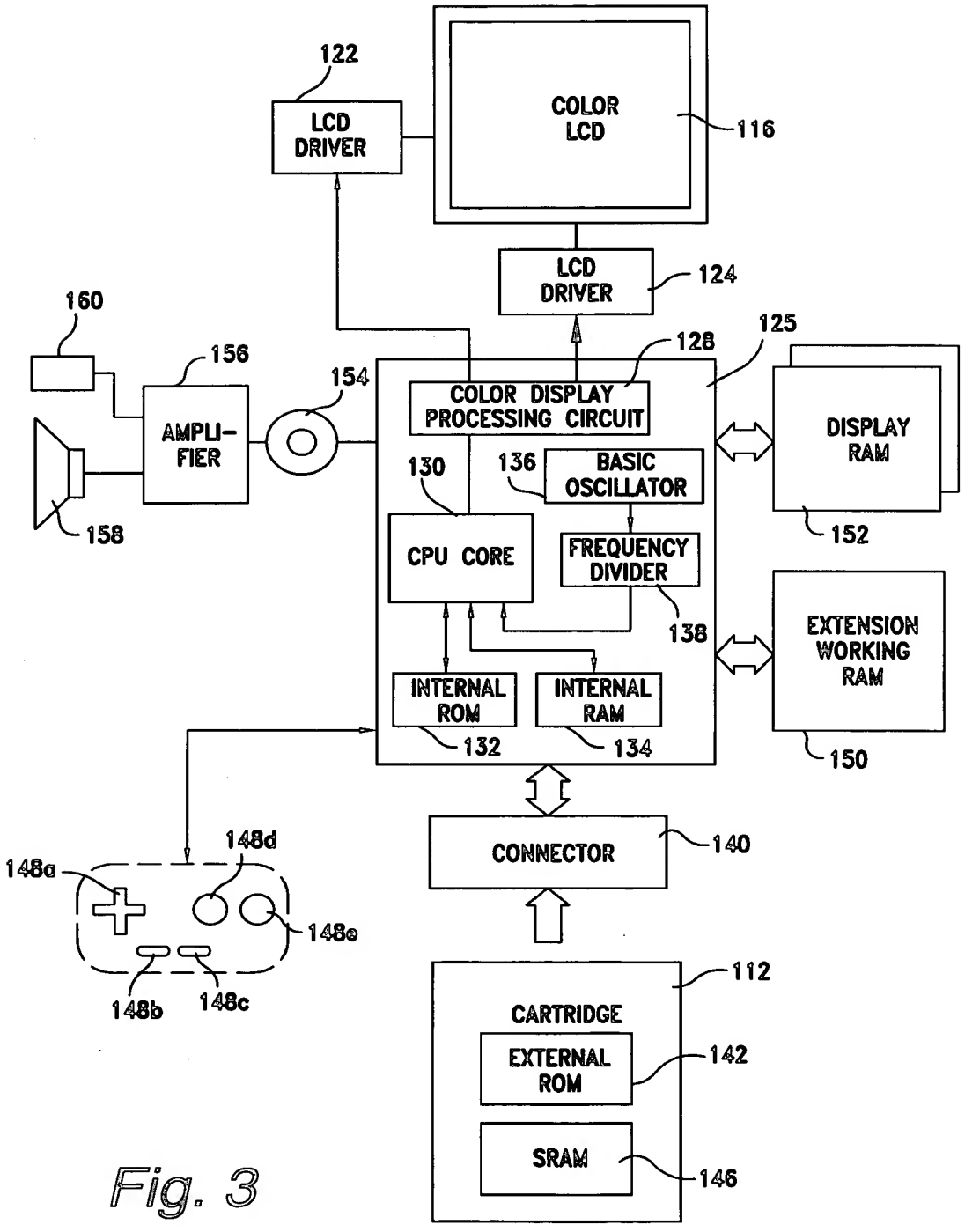

122
LCD DRIVER
COLOR LCD
116
LCD DRIVER
124
160
156
154
125
128
AMPLI-FIER
158
COLOR DISPLAY PROCESSING CIRCUIT
DISPLAY RAM
152
130
136
BASIC OSCILLATOR
CPU CORE
FREQUENCY DIVIDER
138
EXTENSION WORKING RAM
INTERNAL ROM
INTERNAL RAM
132
134
150
148d
148a
CONNECTOR
140
148e
148b
148c
112
CARTRIDGE
EXTERNAL ROM
142
SRAM
146

Fig. 3

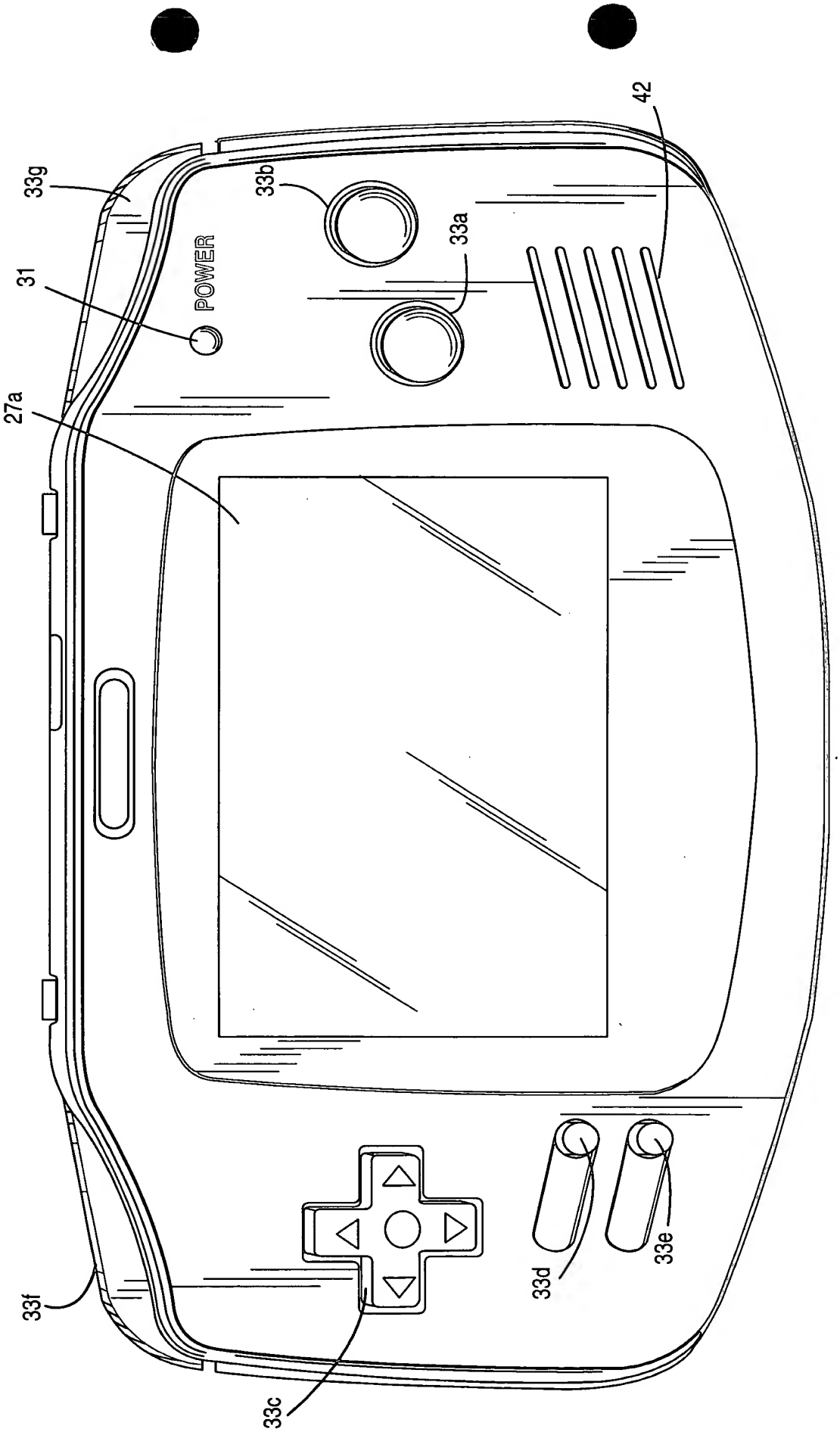


Fig. 4A

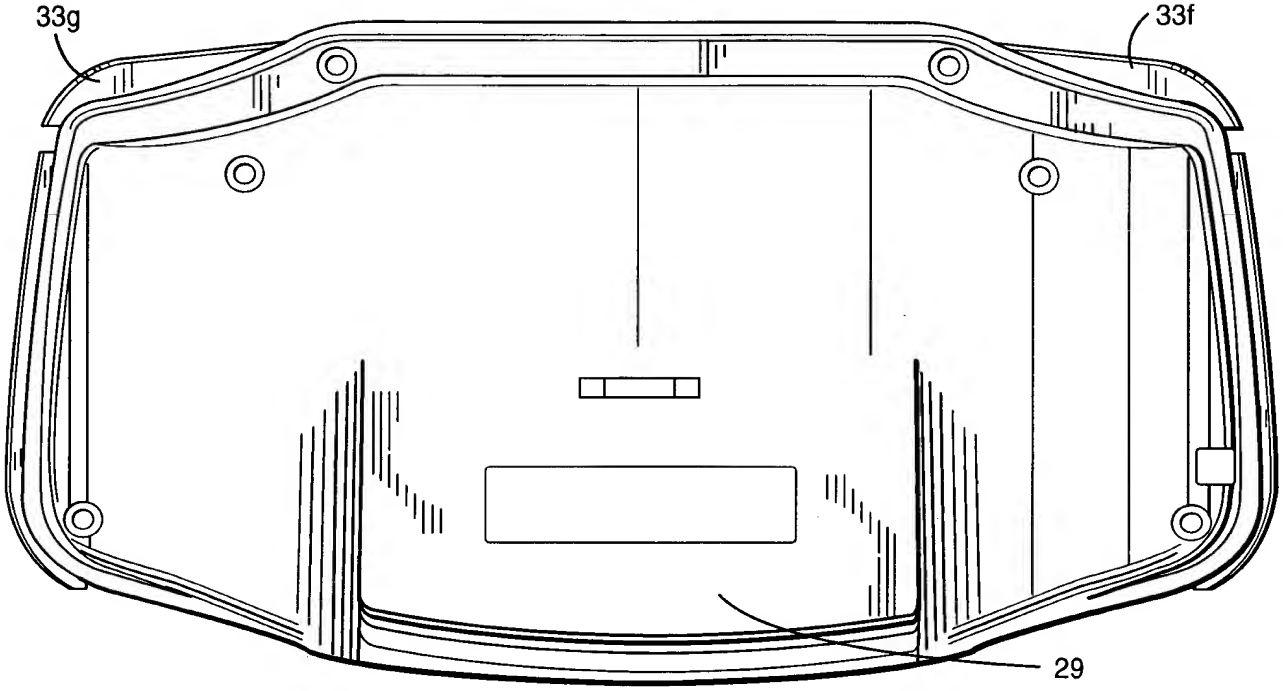


Fig. 4B

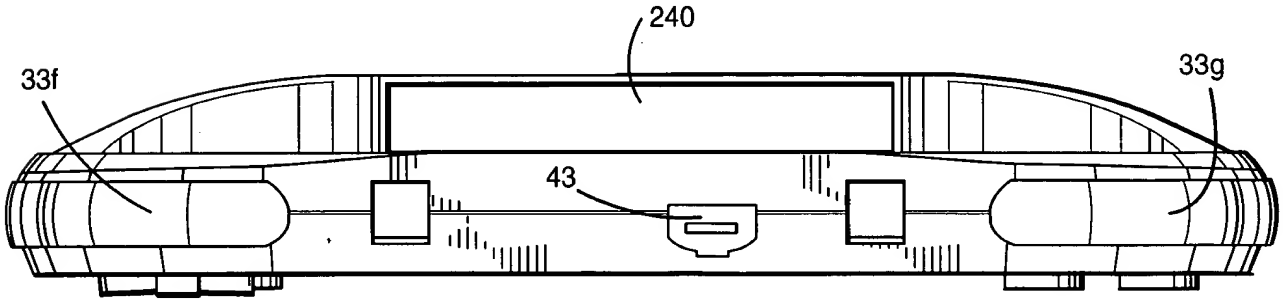


Fig. 4C

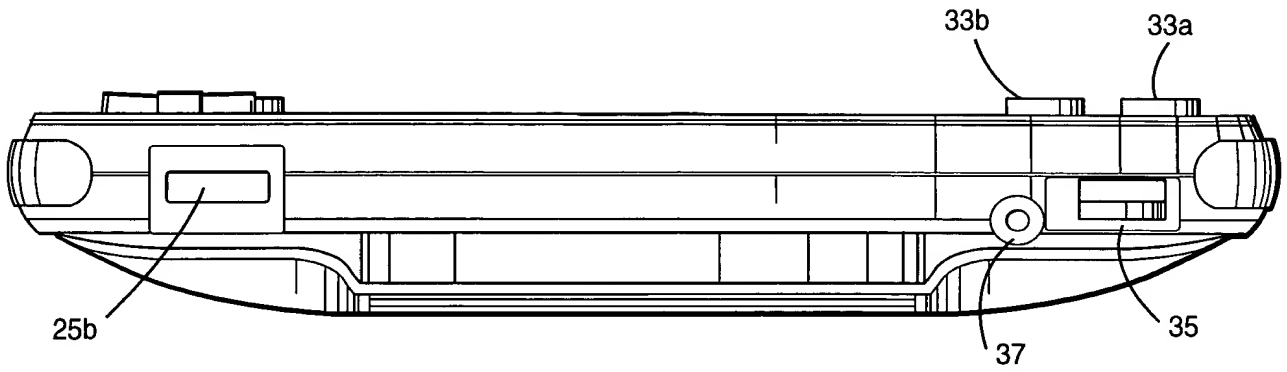


Fig. 4D

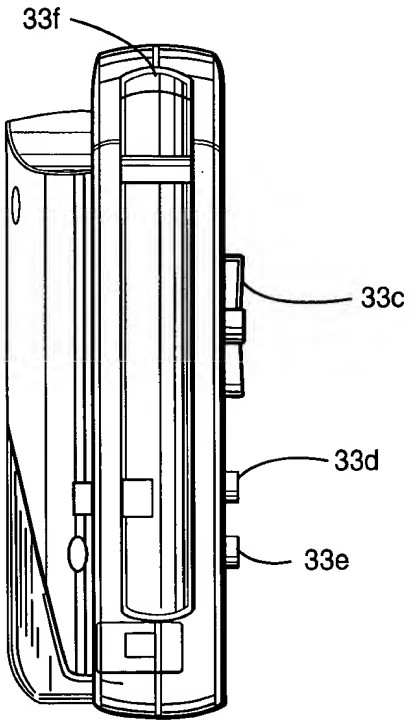


Fig. 4E

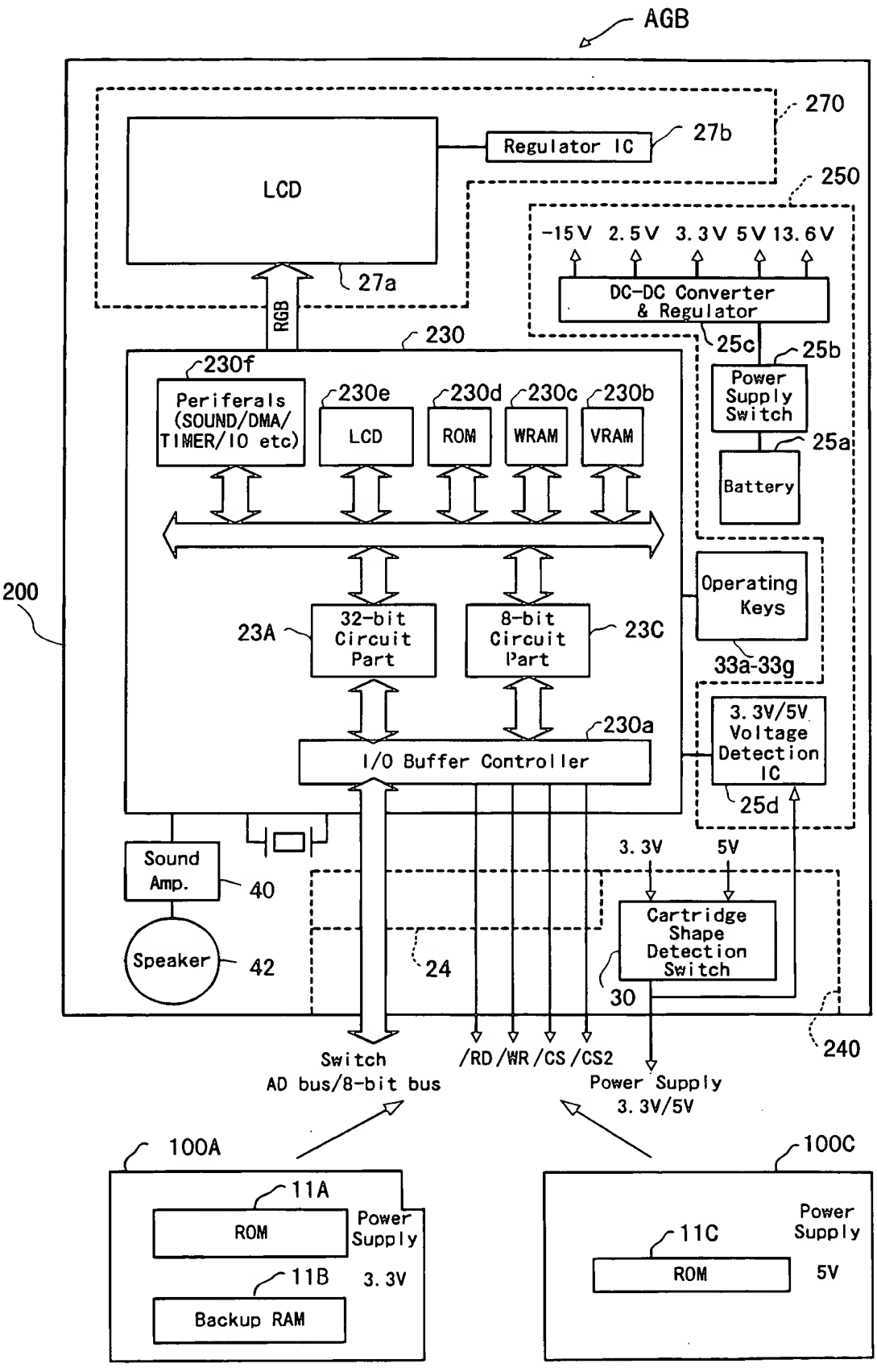

AGB
270
LCD
Regulator IC
27b
250
-15V 2.5V 3.3V 5V 13.6V
27a
RGB
DC-DC Converter & Regulator
25c
25b
230
230f
Periferals (SOUND/DMA/ TIMER/IO etc)
230e
LCD
230d
ROM
230c
WRAM
230b
VRAM
Power Supply Switch
25a
Battery
200
Operating Keys
33a-33g
23A
32-bit Circuit Part
8-bit Circuit Part
23C
3.3V/5V Voltage Detection IC
25d
230a
I/O Buffer Controller
Sound Amp.
40
Speaker
42
24
3.3V
5V
Cartridge Shape Detection Switch
30
240
Switch
AD bus/8-bit bus
/RD /WR /CS /CS2
Power Supply
3.3V/5V
100A
11A
ROM
Power Supply
11B
3.3V
Backup RAM
100C
11C
ROM
Power Supply
5V

Fig. 5A

Fig. 5B

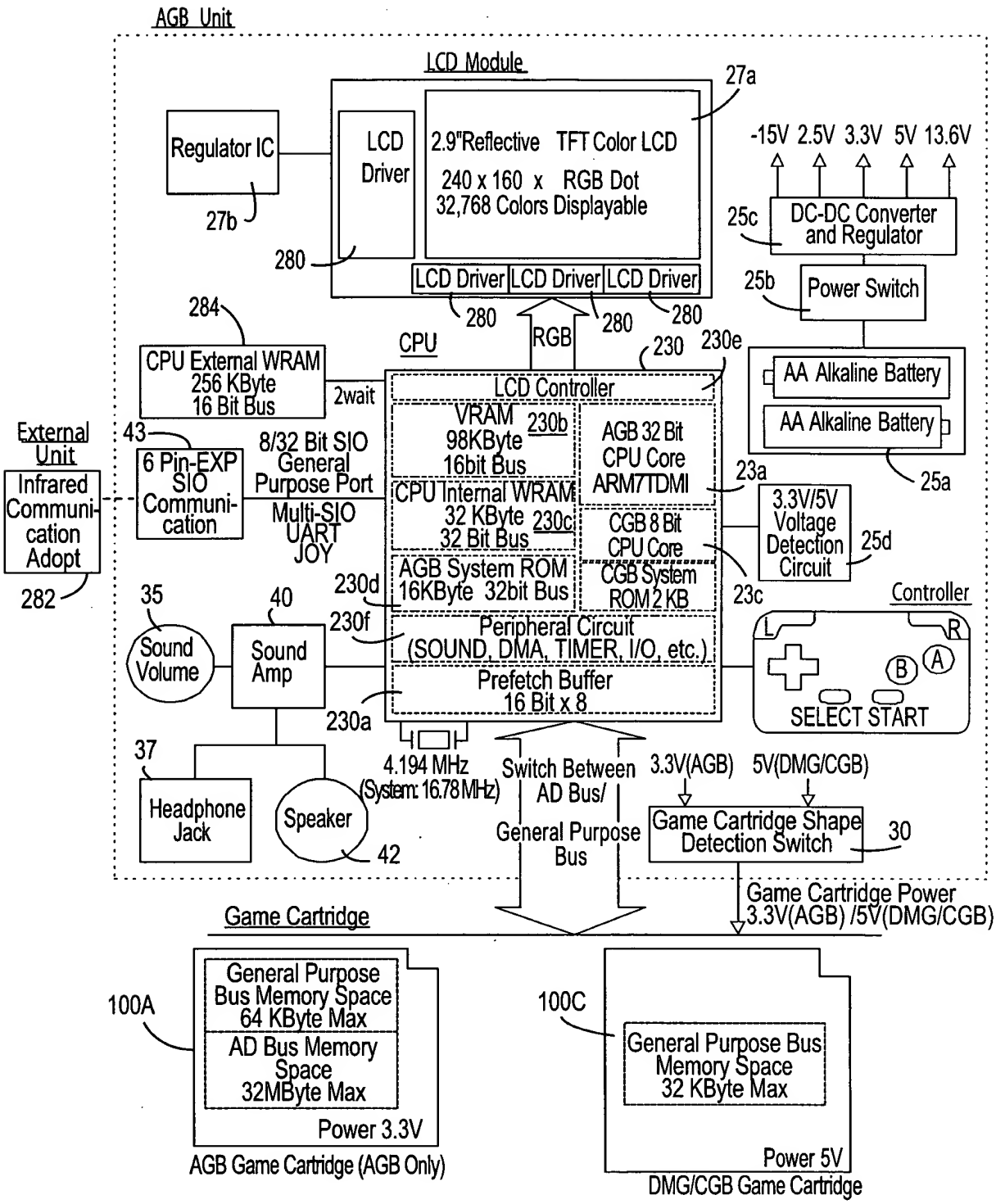
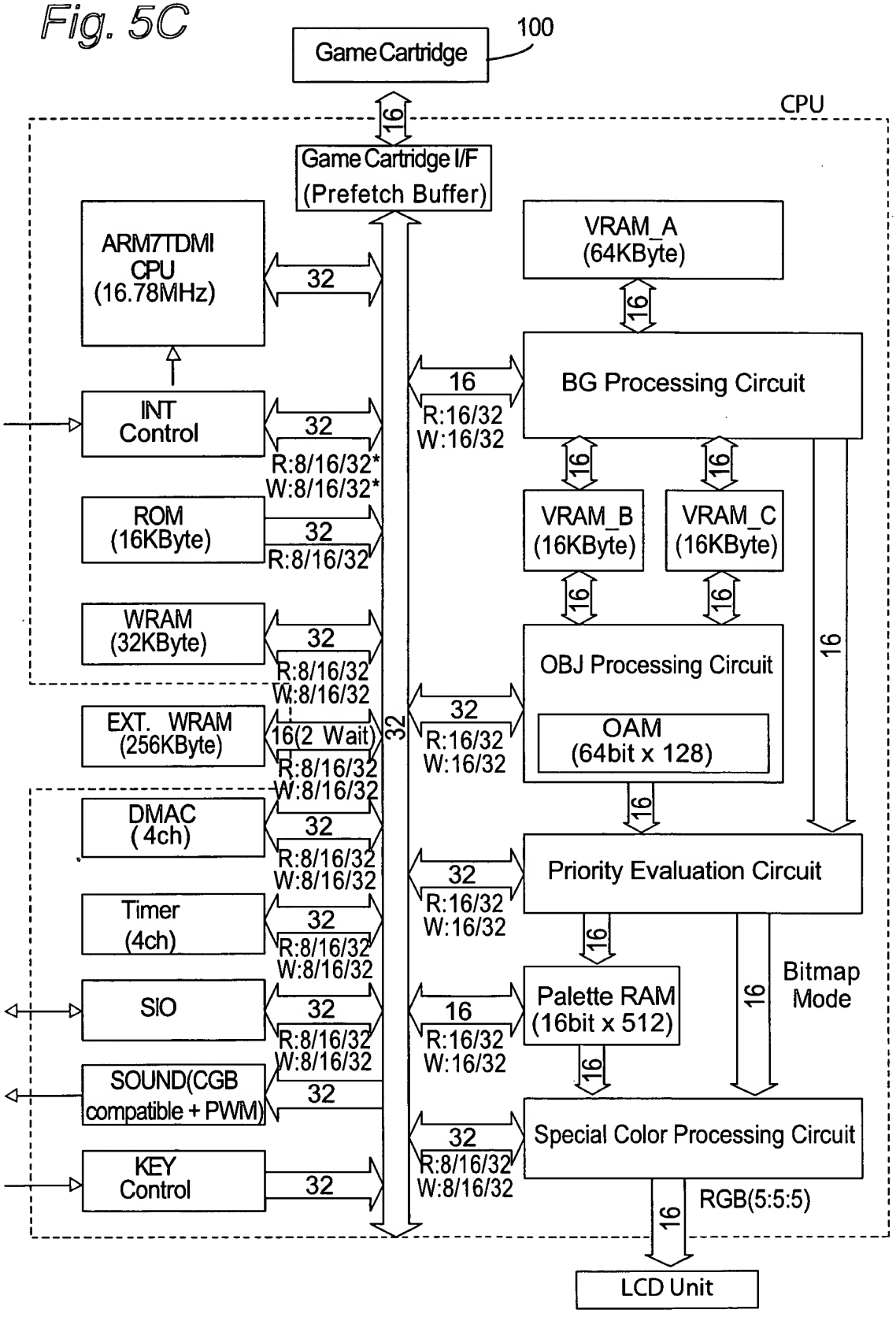

AGB Unit
LCD Module
27a
Regulator IC
27b
LCD Driver
280
2.9"Reflective TFT Color LCD
240 x 160 x RGB Dot
32,768 Colors Displayable
LCD Driver
LCD Driver
LCD Driver
-15V 2.5V 3.3V 5V 13.6V
25c
DC-DC Converter and Regulator
25b
Power Switch
284
CPU External WRAM 256 KByte 16 Bit Bus
2wait
CPU
RGB
230
230e
LCD Controller
VRAM 230b 98KByte 16bit Bus
AGB 32 Bit CPU Core ARM7TDMI
CPU Internal WRAM 32 KByte 230c 32 Bit Bus
CGB 8 Bit CPU Core
AGB System ROM 16KByte 32bit Bus
CGB System ROM 2 KB
Peripheral Circuit (SOUND, DMA, TIMER, I/O, etc.)
Prefetch Buffer 16 Bit x 8
AA Alkaline Battery
AA Alkaline Battery
25a
23a
3.3V/5V Voltage Detection Circuit
25d
23c
Controller
L
R
B
A
SELECT START
External Unit
Infrared Communication Adopt
282
43
6 Pin-EXP SIO Communication
8/32 Bit SIO General Purpose Port
Multi-SIO UART JOY
35
Sound Volume
40
Sound Amp
230d
230f
230a
37
Headphone Jack
Speaker
42
4.194 MHz (System: 16.78 MHz)
Switch Between AD Bus/ General Purpose Bus
3.3V(AGB)
5V(DMG/CGB)
Game Cartridge Shape Detection Switch
30
Game Cartridge Power 3.3V(AGB) /5V(DMG/CGB)
Game Cartridge
100A
General Purpose Bus Memory Space 64 KByte Max
AD Bus Memory Space 32MByte Max
Power 3.3V
AGB Game Cartridge (AGB Only)
100C
General Purpose Bus Memory Space 32 KByte Max
Power 5V
DMG/CGB Game Cartridge

Fig. 5C


Game Cartridge
100
CPU
16
Game Cartridge I/F
(Prefetch Buffer)
ARM7TDMI
CPU
(16.78MHz)
32
INT
Control
32
R:8/16/32*
W:8/16/32*
ROM
(16KByte)
32
R:8/16/32
WRAM
(32KByte)
32
R:8/16/32
W:8/16/32
EXT. WRAM
(256KByte)
16(2 Wait)
R:8/16/32
W:8/16/32
DMAC
(4ch)
32
R:8/16/32
W:8/16/32
Timer
(4ch)
32
R:8/16/32
W:8/16/32
SIO
32
R:8/16/32
W:8/16/32
SOUND(CGB
compatible + PWM)
32
KEY
Control
32
32
VRAM_A
(64KByte)
16
BG Processing Circuit
16
R:16/32
W:16/32
VRAM_B
(16KByte)
VRAM_C
(16KByte)
OBJ Processing Circuit
OAM
(64bit x 128)
32
R:16/32
W:16/32
Priority Evaluation Circuit
32
R:16/32
W:16/32
Palette RAM
(16bit x 512)
16
R:16/32
W:16/32
Special Color Processing Circuit
32
R:8/16/32
W:8/16/32
Bitmap
Mode
RGB(5:5:5)
LCD Unit

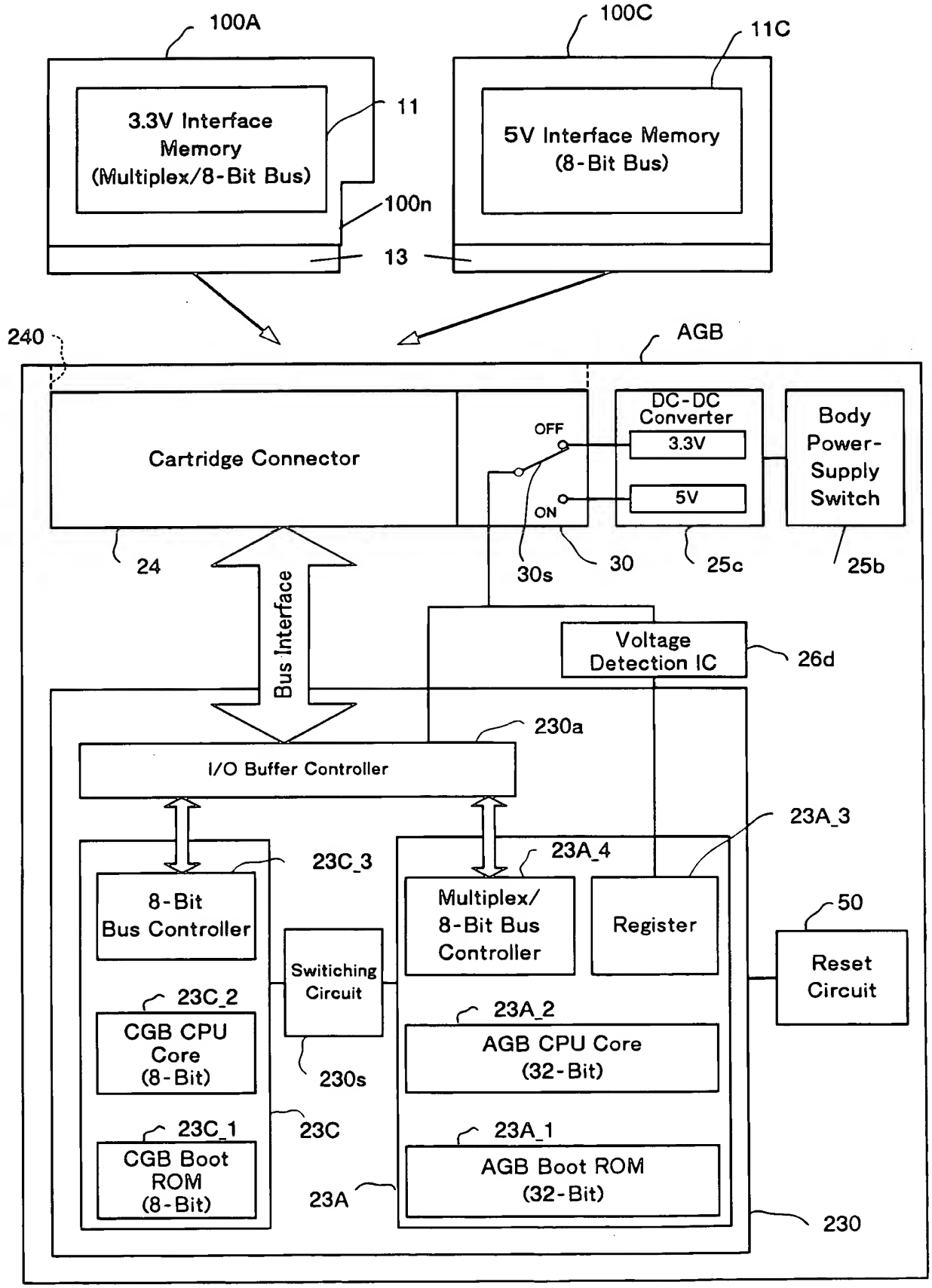

100A
3.3V Interface Memory (Multiplex/8-Bit Bus)
11
100n
13
100C
11C
5V Interface Memory (8-Bit Bus)
240
AGB
Cartridge Connector
OFF
ON
DC-DC Converter
3.3V
5V
Body Power-Supply Switch
24
30s
30
25c
25b
Bus Interface
Voltage Detection IC
26d
230a
I/O Buffer Controller
23A_3
23C_3
23A_4
8-Bit Bus Controller
Multiplex/ 8-Bit Bus Controller
Register
50
Switiching Circuit
Reset Circuit
23C_2
CGB CPU Core (8-Bit)
23A_2
AGB CPU Core (32-Bit)
230s
23C_1
23C
23A_1
CGB Boot ROM (8-Bit)
AGB Boot ROM (32-Bit)
23A
230

Fig. 6

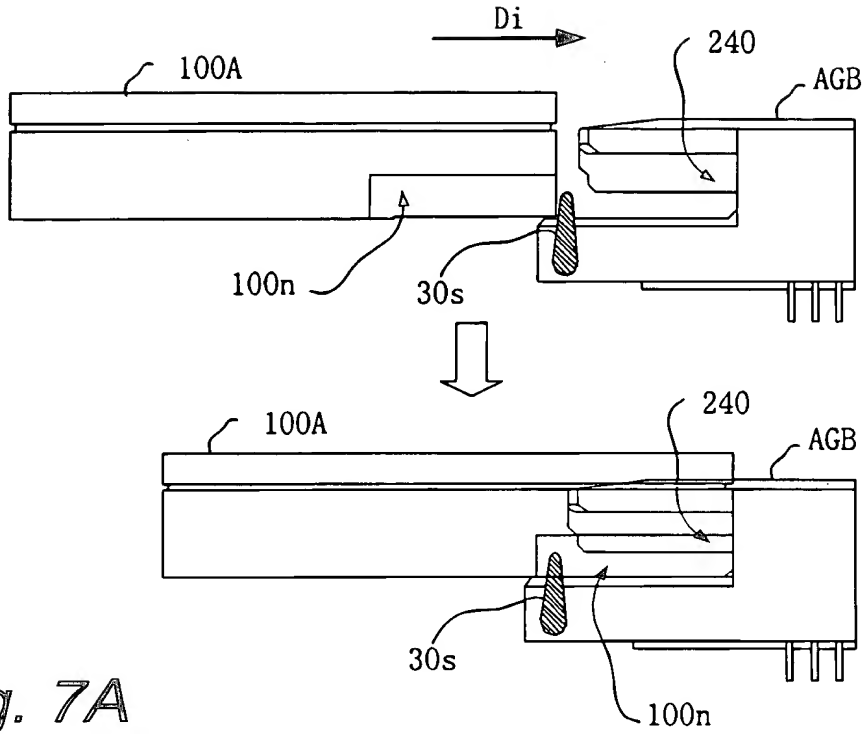

Di
100A
240
AGB
100n
30s
100A
240
AGB
30s
100n

Fig. 7A

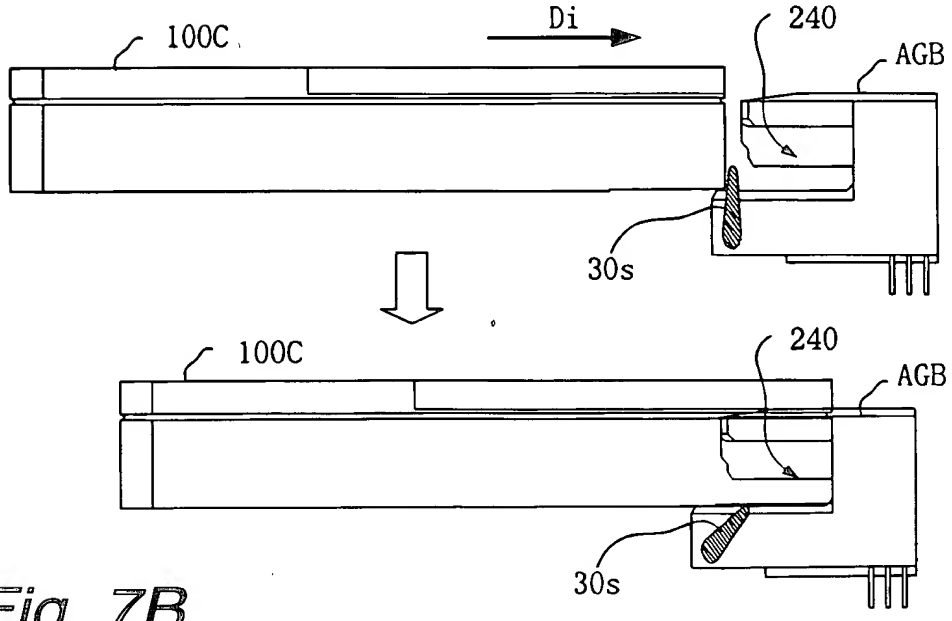

Di
100C
240
AGB
30s
100C
240
AGB
30s

Fig. 7B

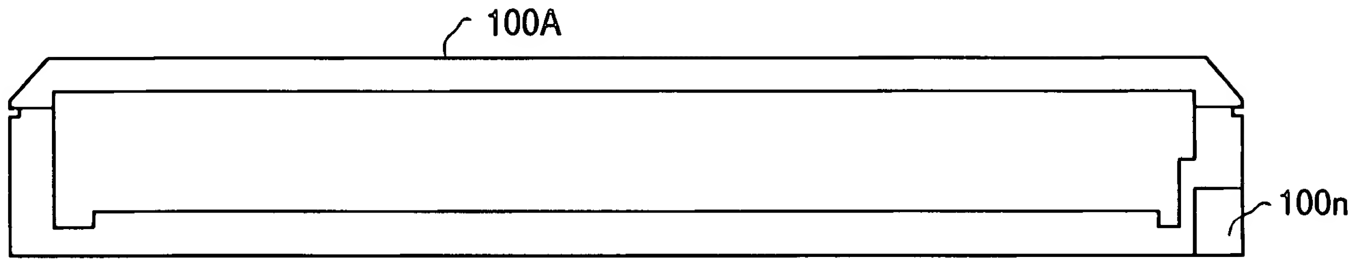


Fig. 8A

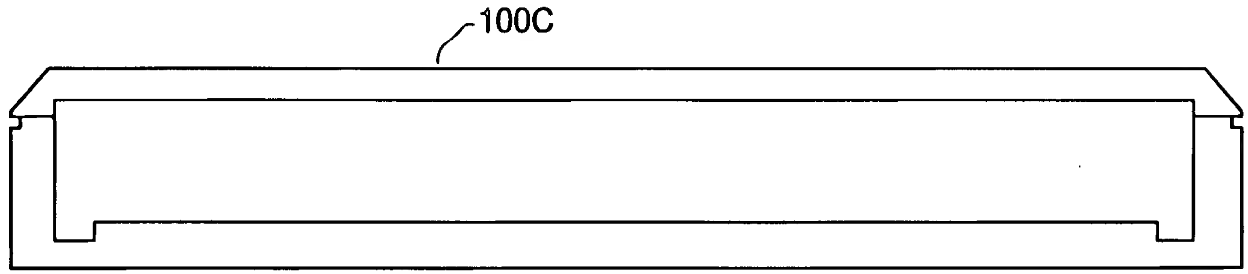


Fig. 8B

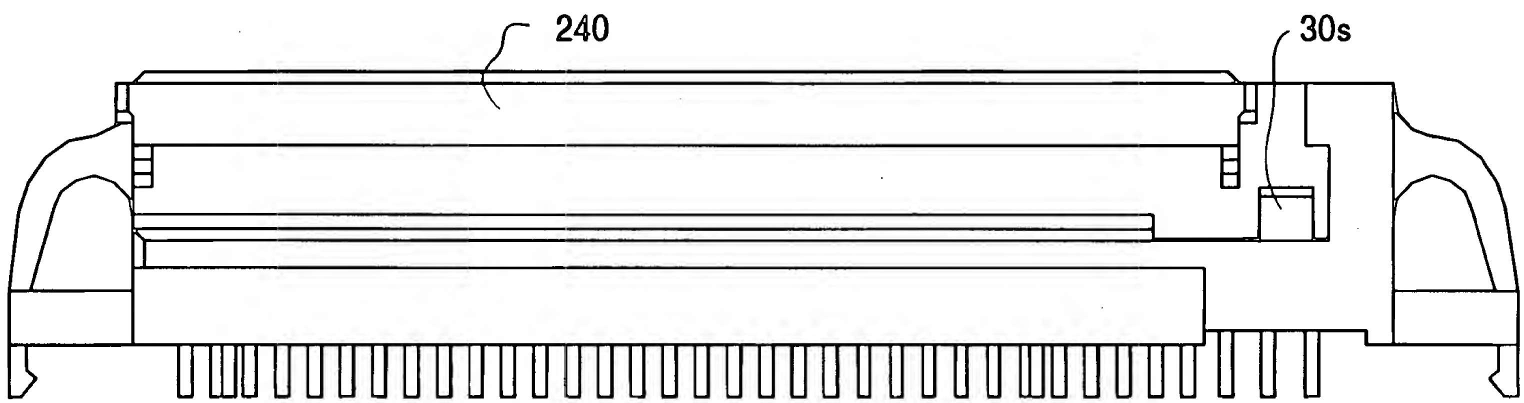


Fig. 8C

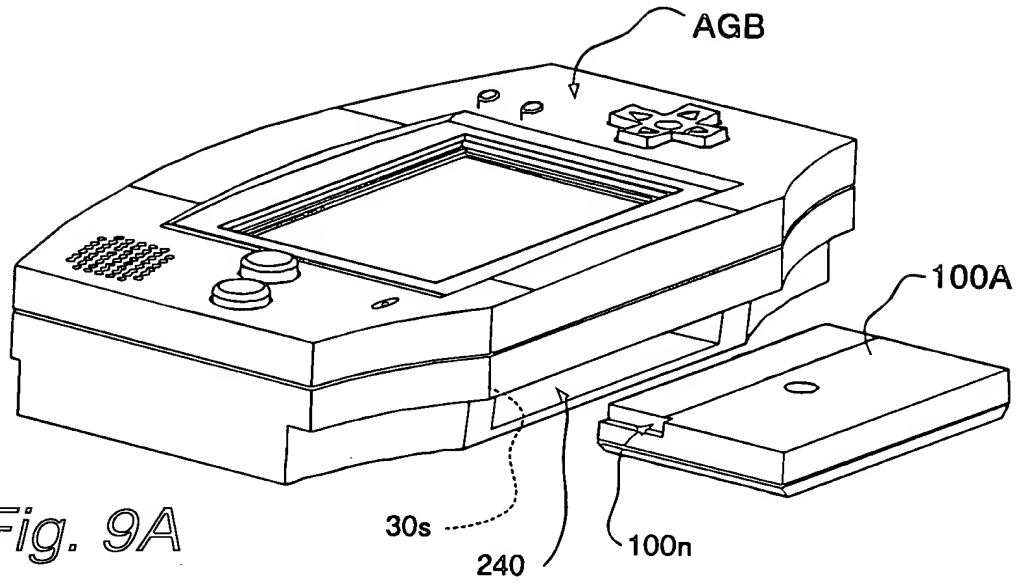


Fig. 9A

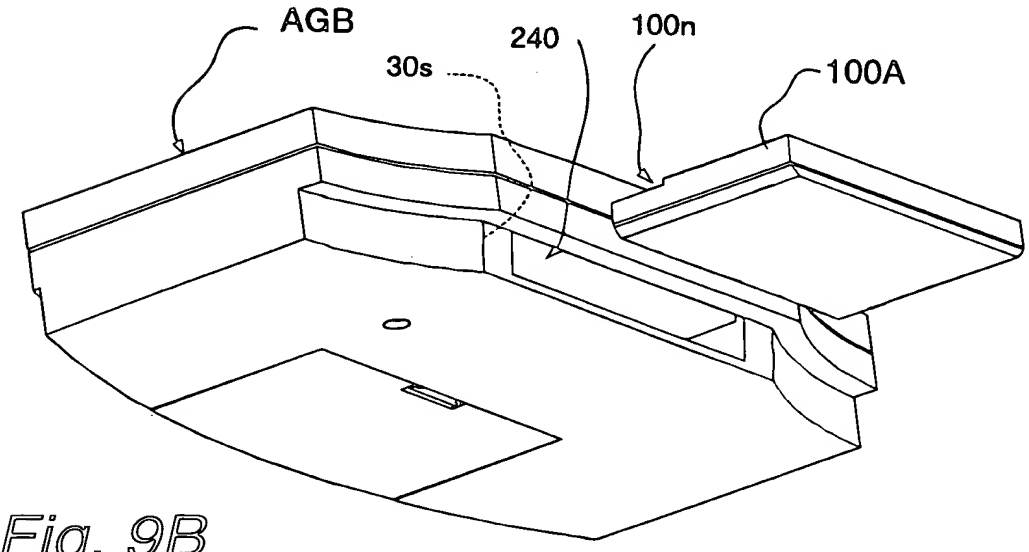


Fig. 9B

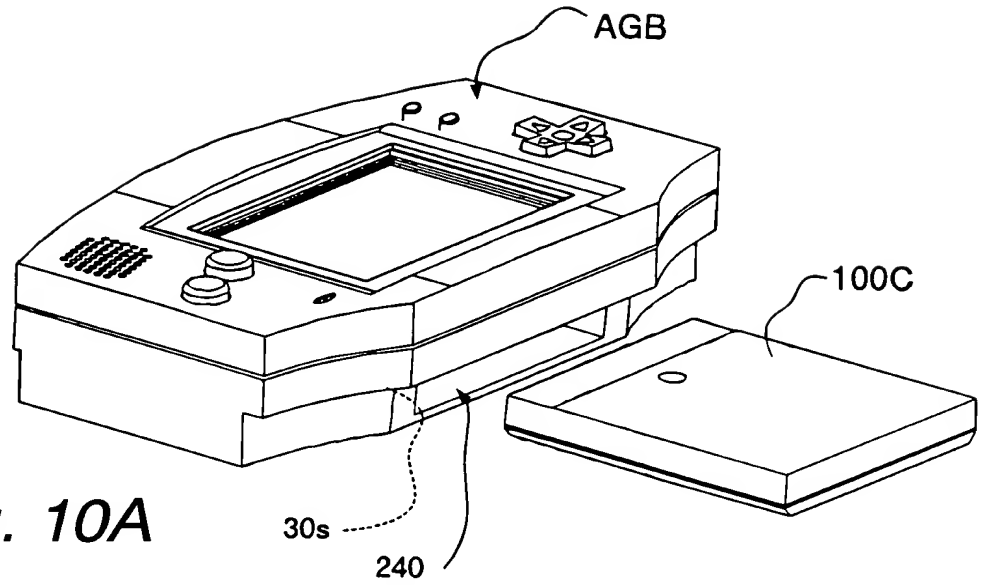


Fig. 10A

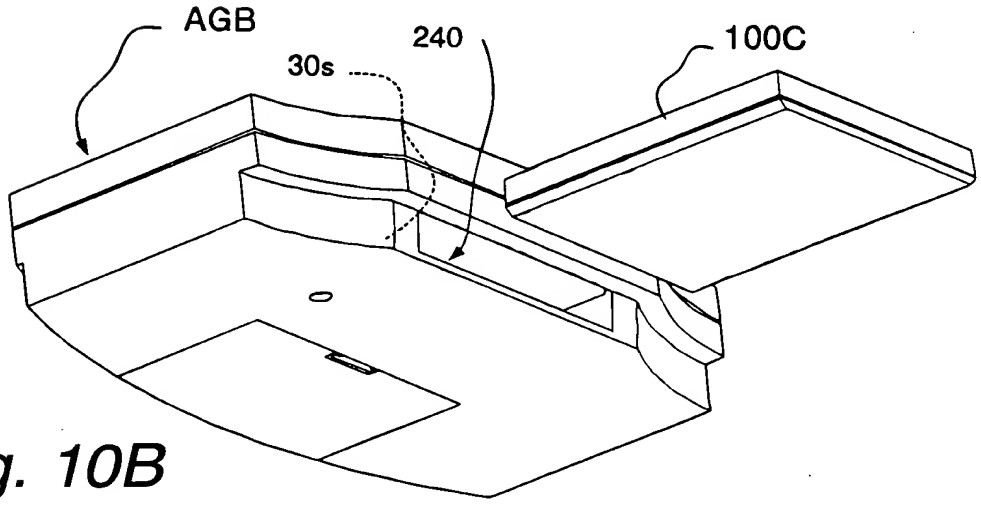


Fig. 10B

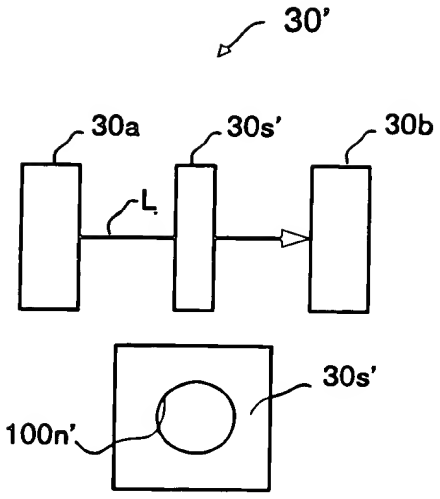


Fig. 11A

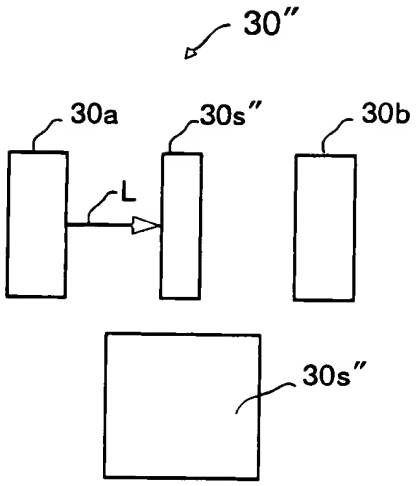


Fig. 11B

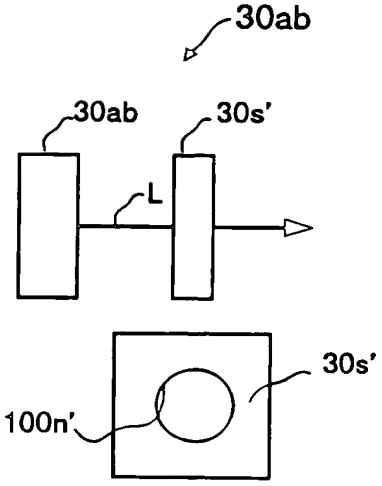


Fig. 11C

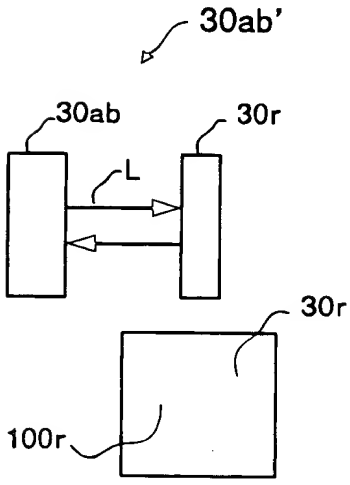


Fig. 11D

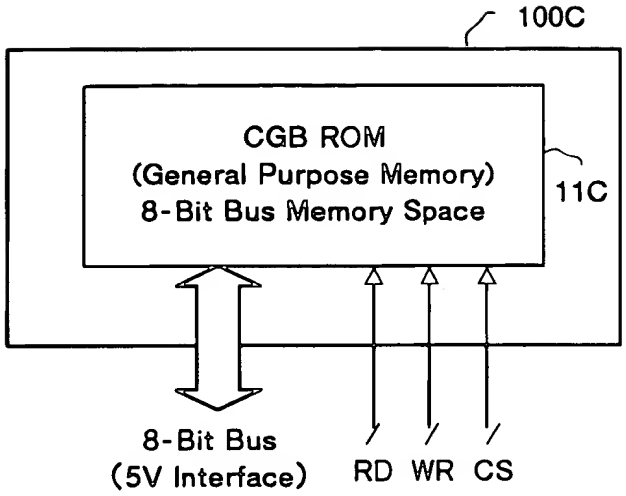


Fig. 12A

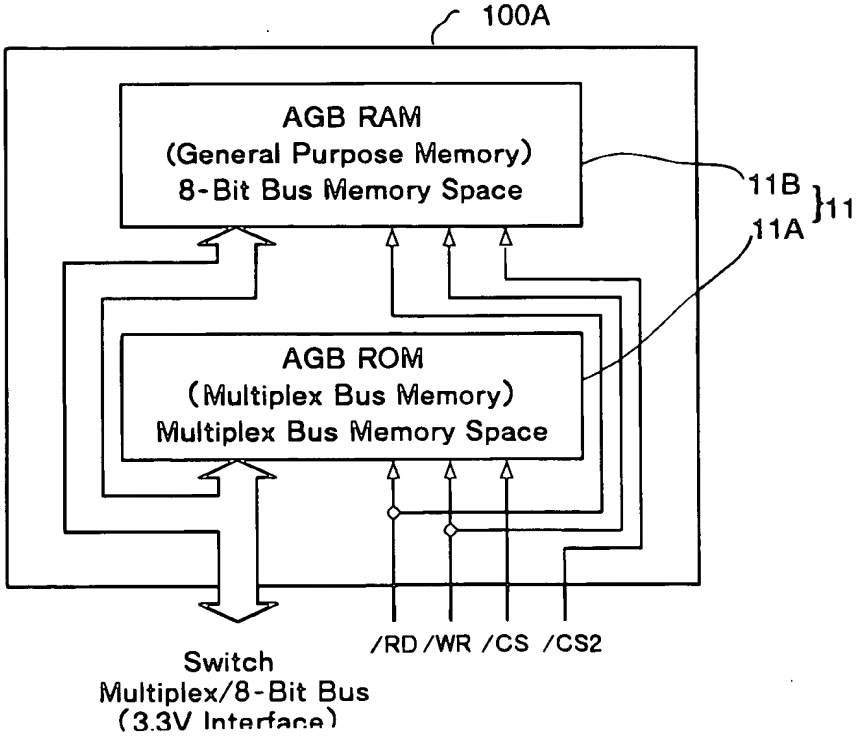


Fig. 12B

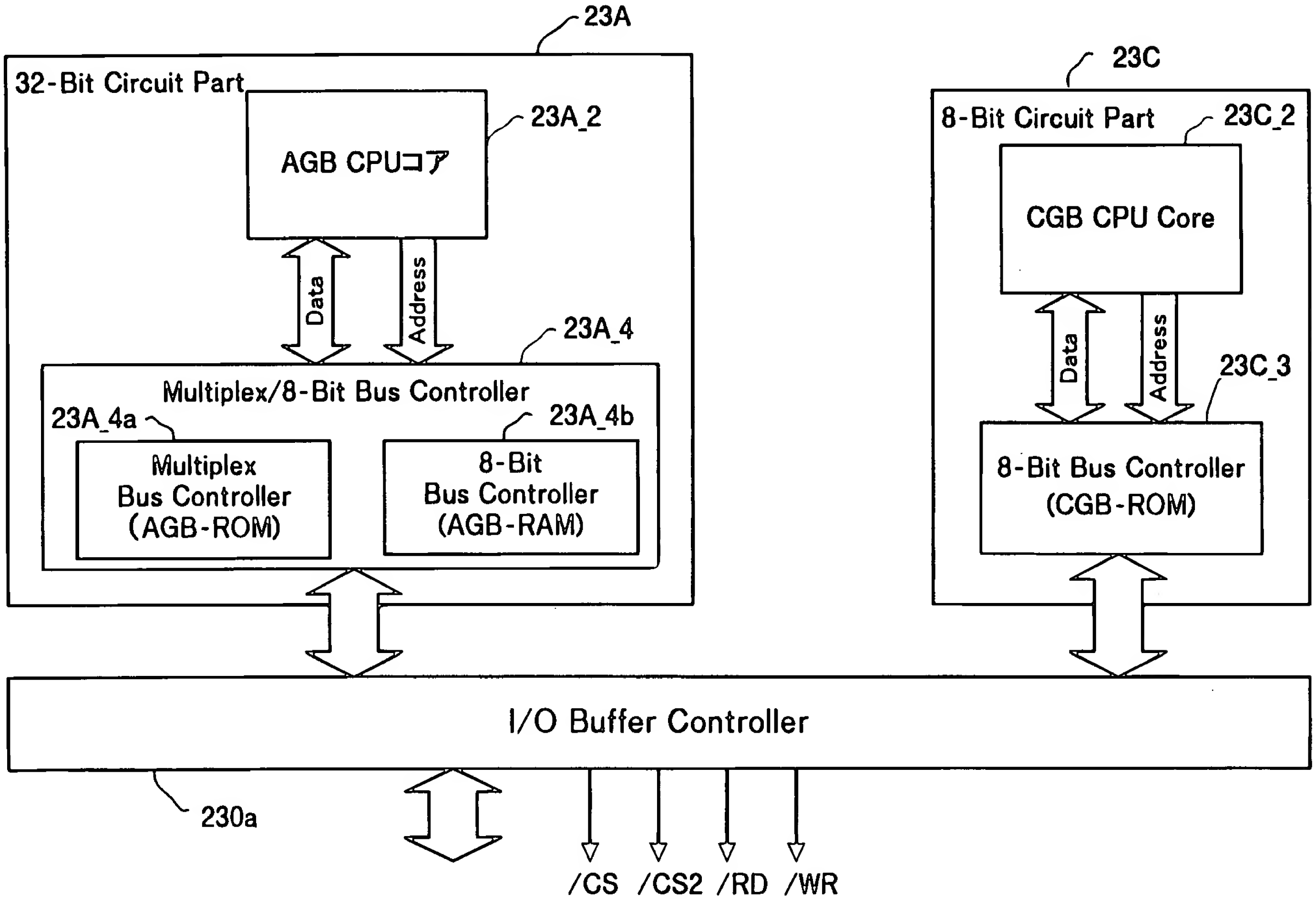

23A
32-Bit Circuit Part
AGB CPUコア
23A_2
Data
Address
23A_4
Multiplex/8-Bit Bus Controller
23A_4a
Multiplex
Bus Controller
(AGB-ROM)
23A_4b
8-Bit
Bus Controller
(AGB-RAM)
23C
8-Bit Circuit Part
23C_2
CGB CPU Core
Data
Address
23C_3
8-Bit Bus Controller
(CGB-ROM)
I/O Buffer Controller
230a
/CS /CS2 /RD /WR

Fig. 13

Fig. 14

NO	CGB	AGB ROM	AGB RAM	Remarks
1	VDD(5V)	VDD(3.3V)	VDD(3.3V)	Switch Voltage By Detection Switch
2	PHI	PHI	PHI	
3	/WR	/WR	/WR	
4	/RD	/RD	/RD	
5	/CS	/CS	/CS	Select ROM Chip
6	A0	A0/DO	A0	Address/Data Shared Terminal
7	A1	A1/D1	A1	Same As Above
8	A2	A2/D2	A2	Same As Above
9	A3	A3/D3	A3	Same As Above
10	A4	A4/D4	A4	Same As Above
11	A5	A5/D5	A5	Same As Above
12	A6	A6/D6	A6	Same As Above
13	A7	A7/D7	A7	Same As Above
14	A8	A8/D8	A8	Same As Above
15	A9	A9/D9	A9	Same As Above
16	A10	A10/D10	A10	Same As Above
17	A11	A11/D11	A11	Same As Above
18	A12	A12/D12	A12	Same As Above
19	A13	A13/D13	A13	Same As Above
20	A14	A14/D14	A14	Same As Above
21	A15	A15/D15	A15	Same As Above
22	D0	A16	D0	
23	D1	A17	D1	
24	D2	A18	D2	
25	D3	A19	D3	
26	D4	A20	D4	
27	D5	A21	D5	
28	D6	A22	D6	
29	D7	A23	D7	
30	/RES	/CS2	/CS2	Action Each Different In AGB and CGB Modes
31	Not Allowed to Use (VIN)	IREQ/ DREQ	IREQ/ DREQ	In CGB Mode, Ignore VIN Input
32	GND	GND	GND	

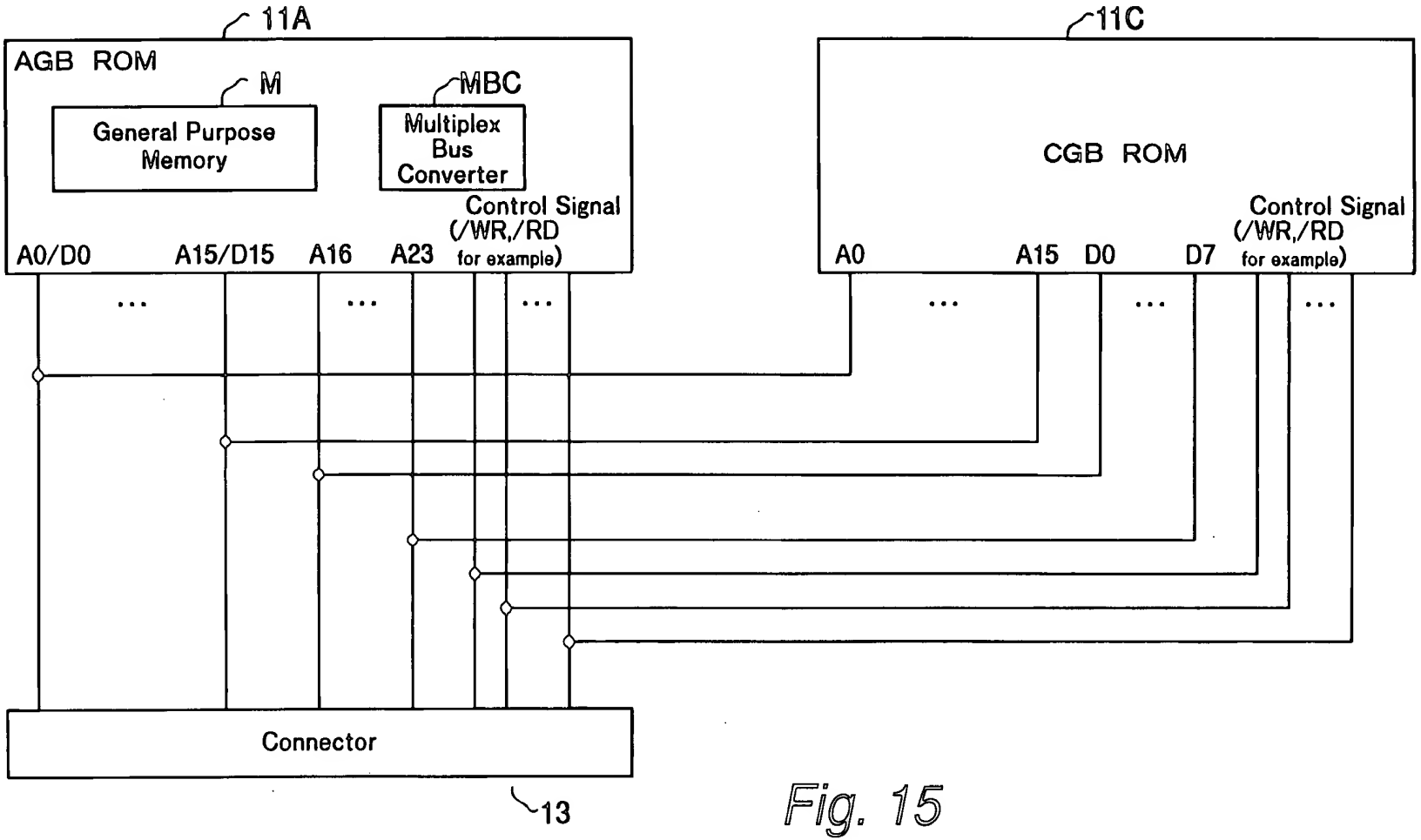


Fig. 15

Fig. 16A

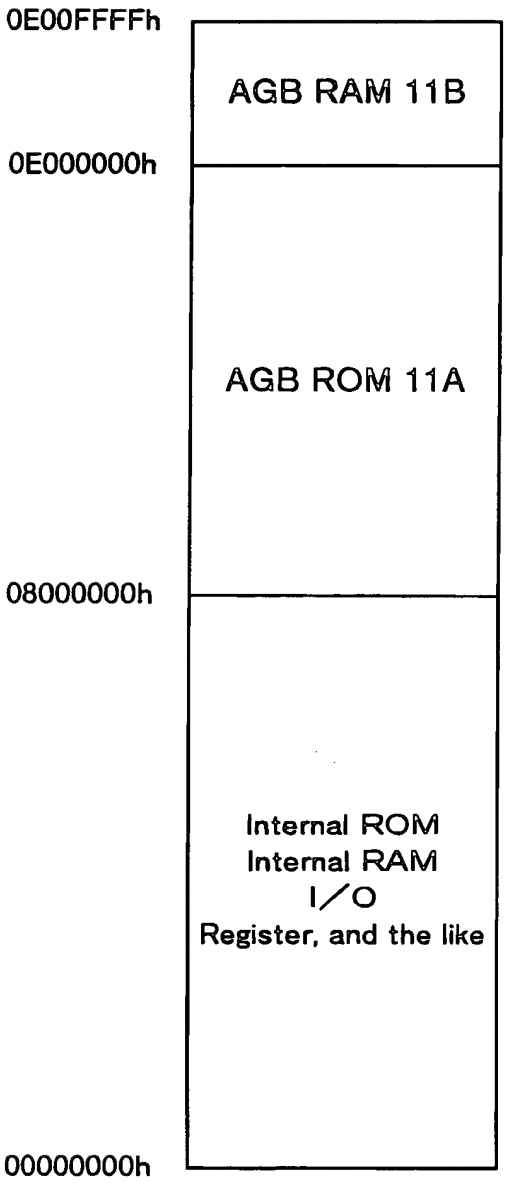


Fig. 16C

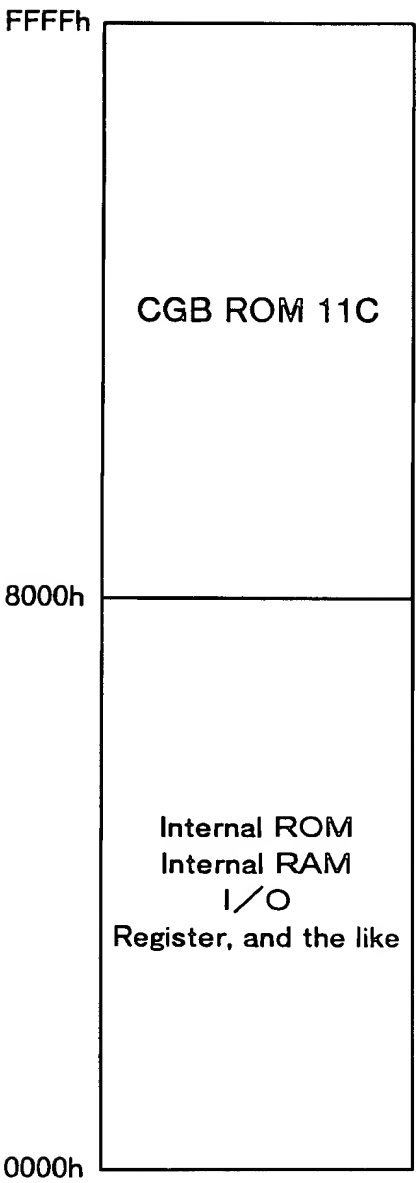


Fig. 16B

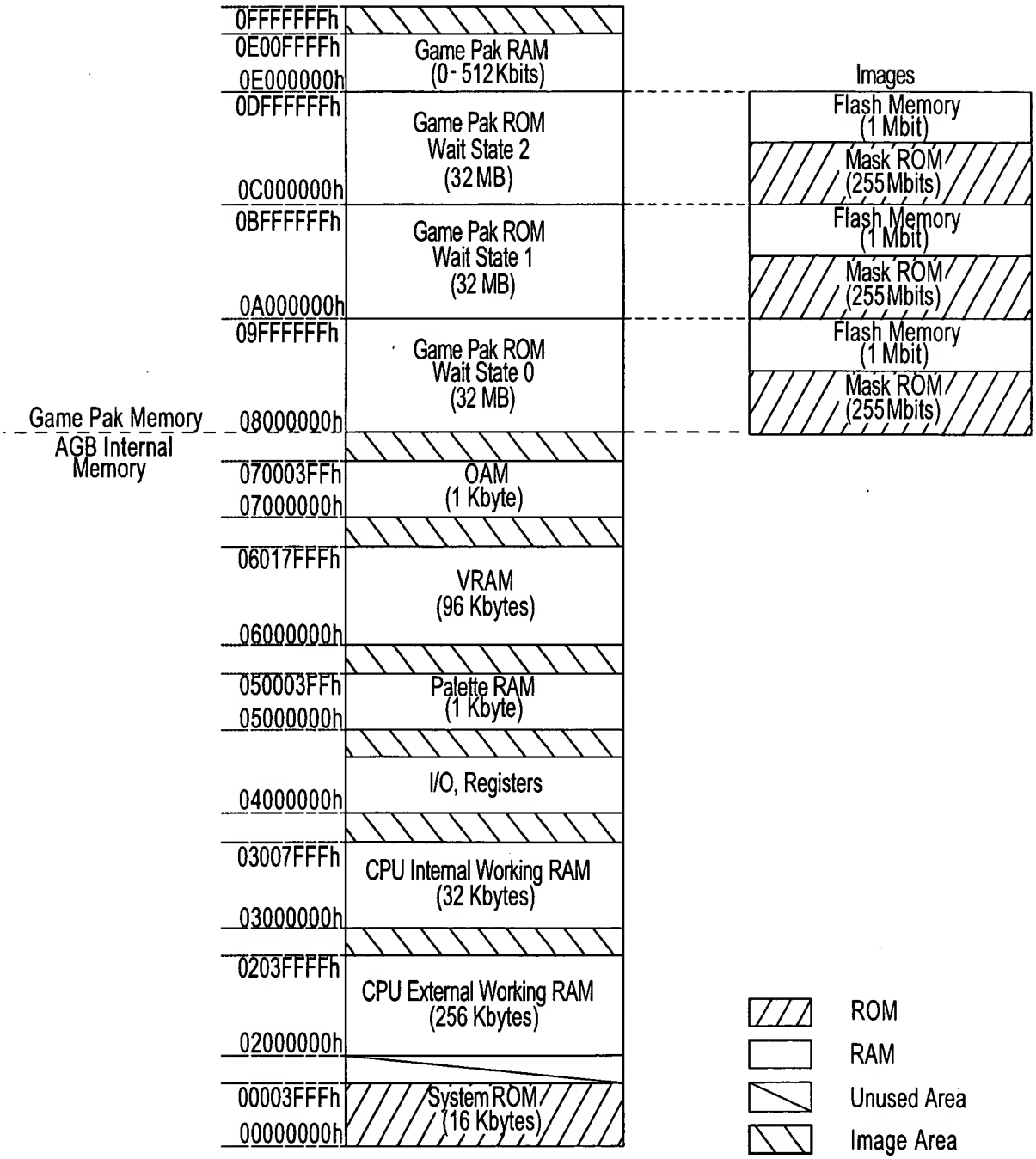
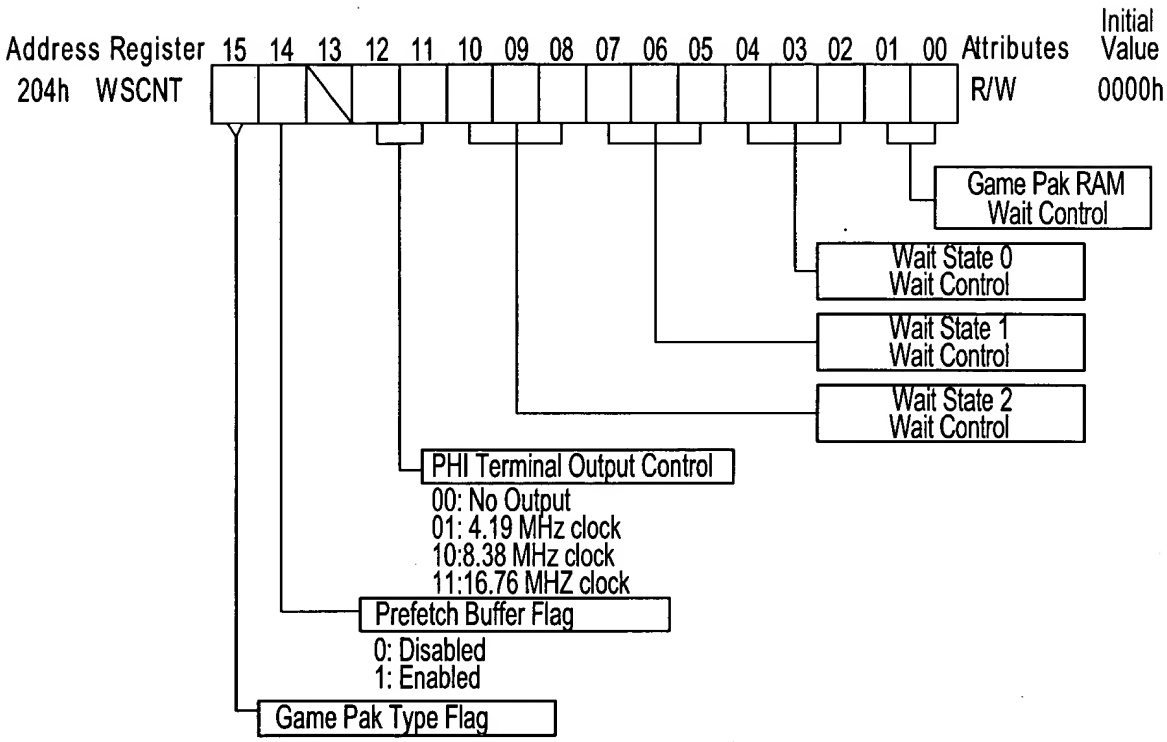

0FFFFFFFh
0E00FFFFh
0E000000h
Game Pak RAM
(0-512Kbits)
0DFFFFFFh
Game Pak ROM
Wait State 2
(32MB)
0C000000h
0BFFFFFFh
Game Pak ROM
Wait State 1
(32 MB)
0A000000h
09FFFFFFh
Game Pak ROM
Wait State 0
(32 MB)
08000000h
Game Pak Memory
AGB Internal
Memory
070003FFh
07000000h
OAM
(1 Kbyte)
06017FFFh
VRAM
(96 Kbytes)
06000000h
050003FFh
05000000h
Palette RAM
(1 Kbyte)
I/O, Registers
04000000h
03007FFFh
CPU Internal Working RAM
(32 Kbytes)
03000000h
0203FFFFh
CPU External Working RAM
(256 Kbytes)
02000000h
00003FFFh
00000000h
System ROM
(16 Kbytes)
Images
Flash Memory
(1 Mbit)
Mask ROM
(255Mbits)
Flash Memory
(1 Mbit)
Mask ROM
(255Mbits)
Flash Memory
(1 Mbit)
Mask ROM
(255Mbits)
ROM
RAM
Unused Area
Image Area

Fig. 17


Address Register
204h WSCNT
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Attributes
R/W
Initial Value
0000h
Game Pak RAM Wait Control
Wait State 0 Wait Control
Wait State 1 Wait Control
Wait State 2 Wait Control
PHI Terminal Output Control
00: No Output
01: 4.19 MHz clock
10:8.38 MHz clock
11:16.76 MHZ clock
Prefetch Buffer Flag
0: Disabled
1: Enabled
Game Pak Type Flag

AGB ROM11A Read Access

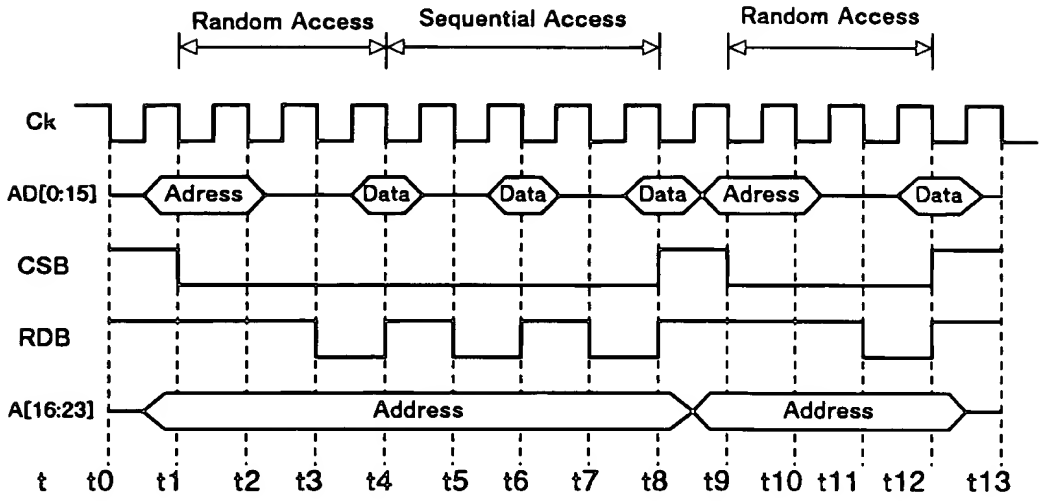


Fig. 18A

AGB RAM11B Write Access

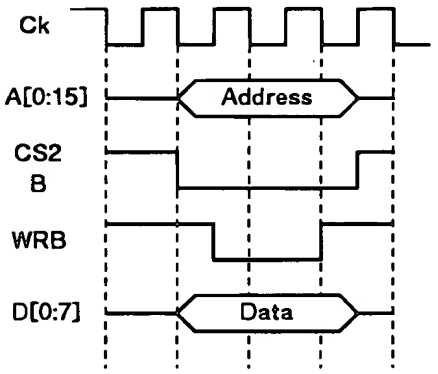


Fig. 18D

AGB RAM11B Read Access

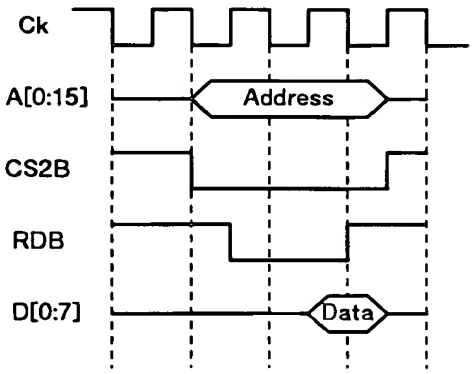


Fig. 18E

CGB ROM11C Read Access

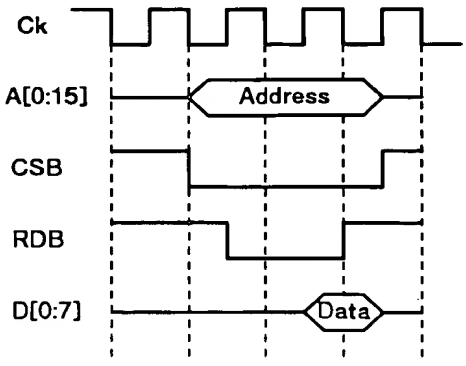


Fig. 18F

Fig. 18B

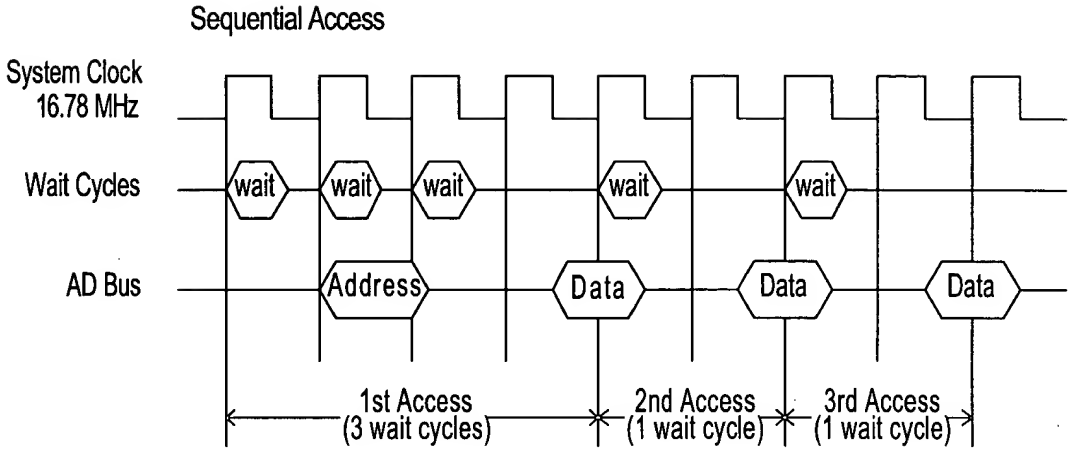
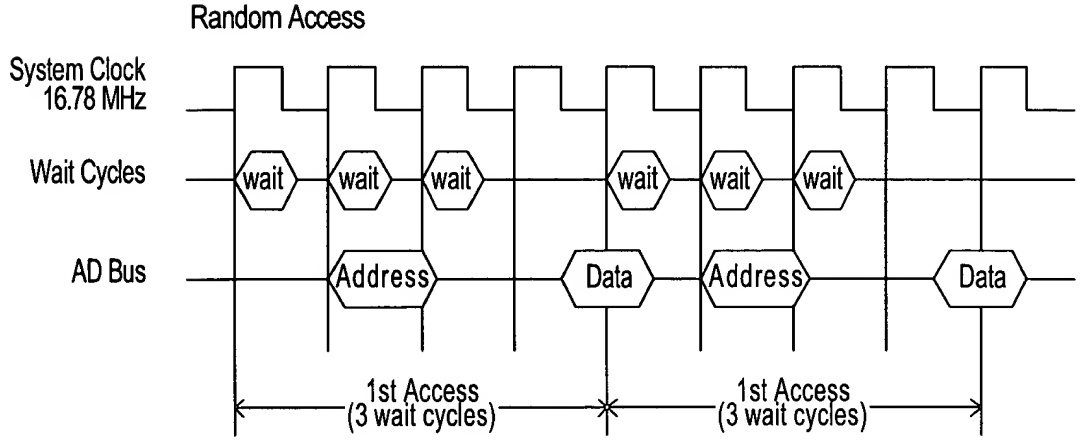


Fig. 18C



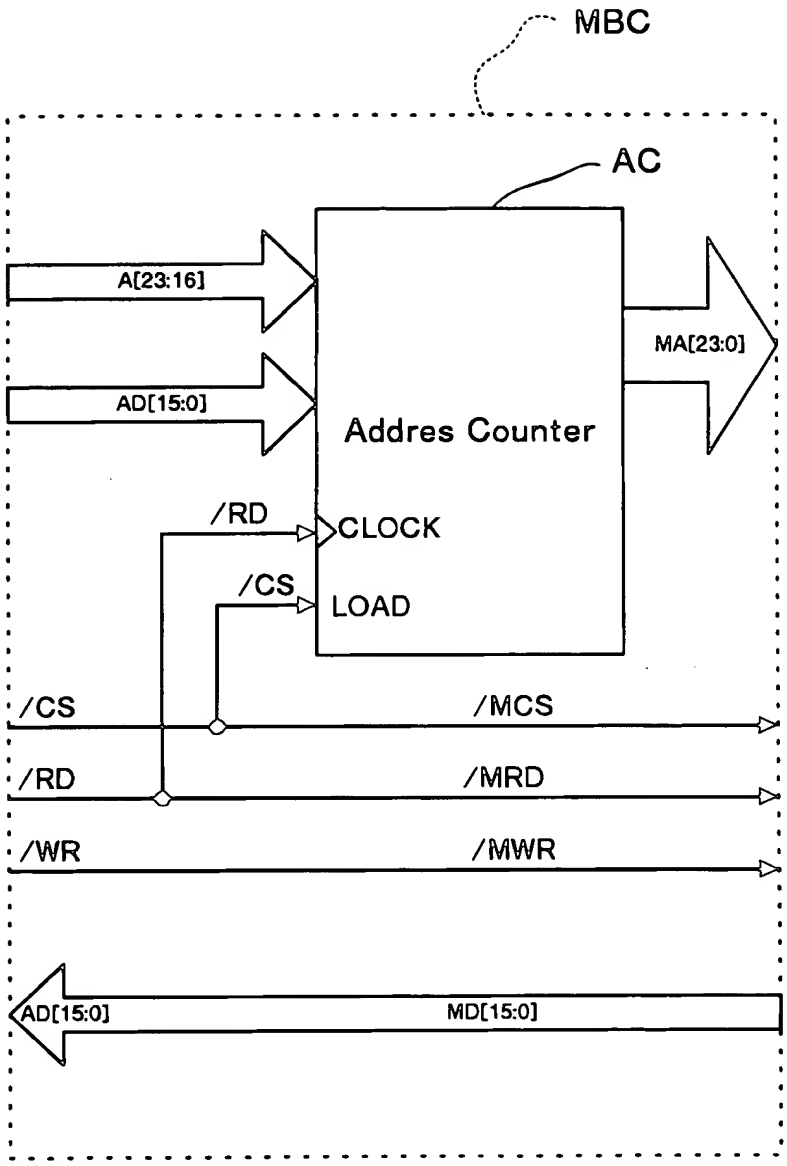

MBC
AC
A[23:16]
AD[15:0]
Addres Counter
MA[23:0]
/RD
CLOCK
/CS
LOAD
/CS
/MCS
/RD
/MRD
/WR
/MWR
AD[15:0]
MD[15:0]

Fig. 19

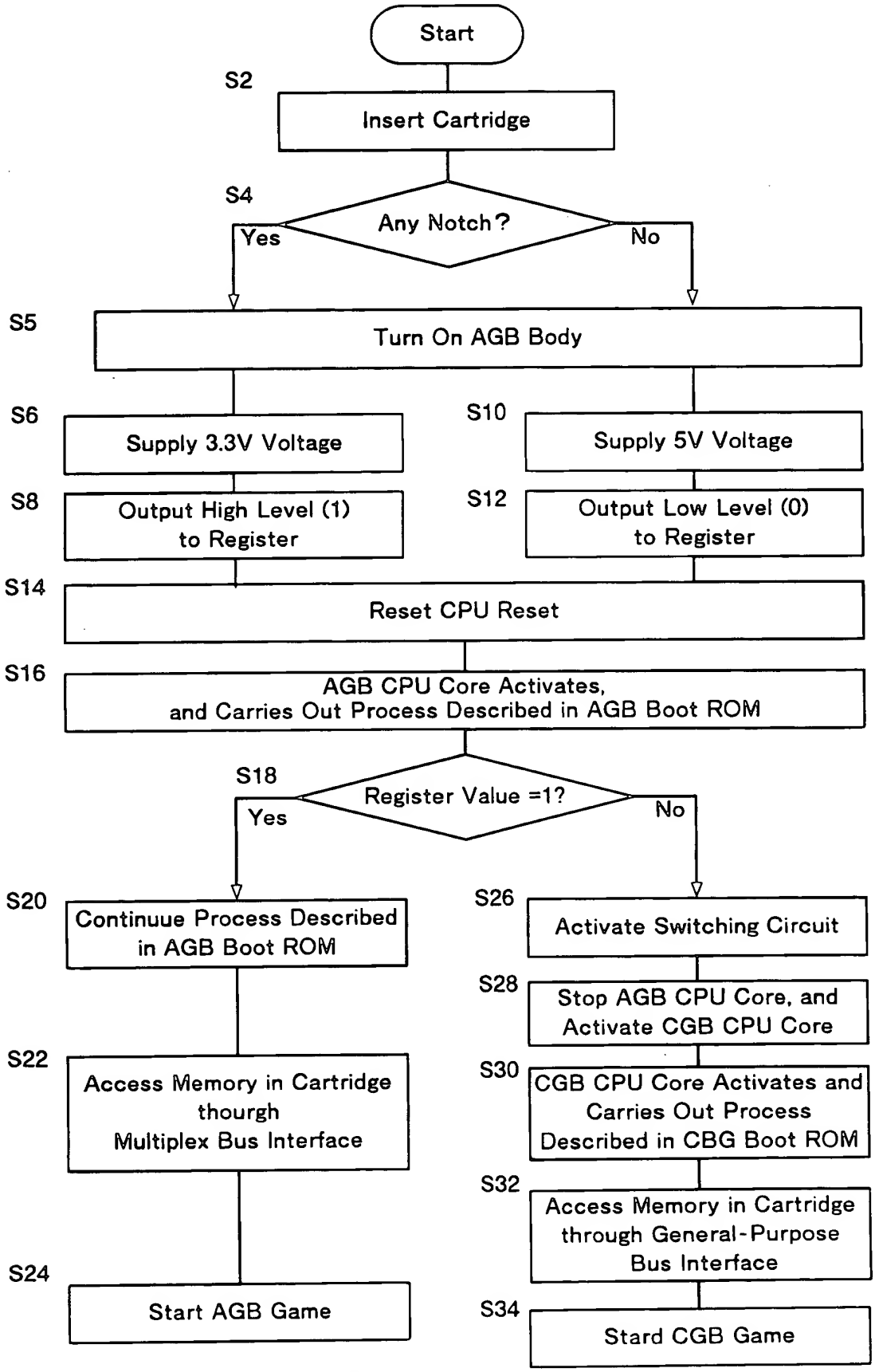

Start
S2
Insert Cartridge
S4
Any Notch?
Yes
No
S5
Turn On AGB Body
S6
Supply 3.3V Voltage
S8
Output High Level (1) to Register
S10
Supply 5V Voltage
S12
Output Low Level (0) to Register
S14
Reset CPU Reset
S16
AGB CPU Core Activates, and Carries Out Process Described in AGB Boot ROM
S18
Register Value =1?
Yes
No
S20
Continuue Process Described in AGB Boot ROM
S22
Access Memory in Cartridge thourgh Multiplex Bus Interface
S24
Start AGB Game
S26
Activate Switching Circuit
S28
Stop AGB CPU Core, and Activate CGB CPU Core
S30
CGB CPU Core Activates and Carries Out Process Described in CBG Boot ROM
S32
Access Memory in Cartridge through General-Purpose Bus Interface
S34
Stard CGB Game

Fig. 20

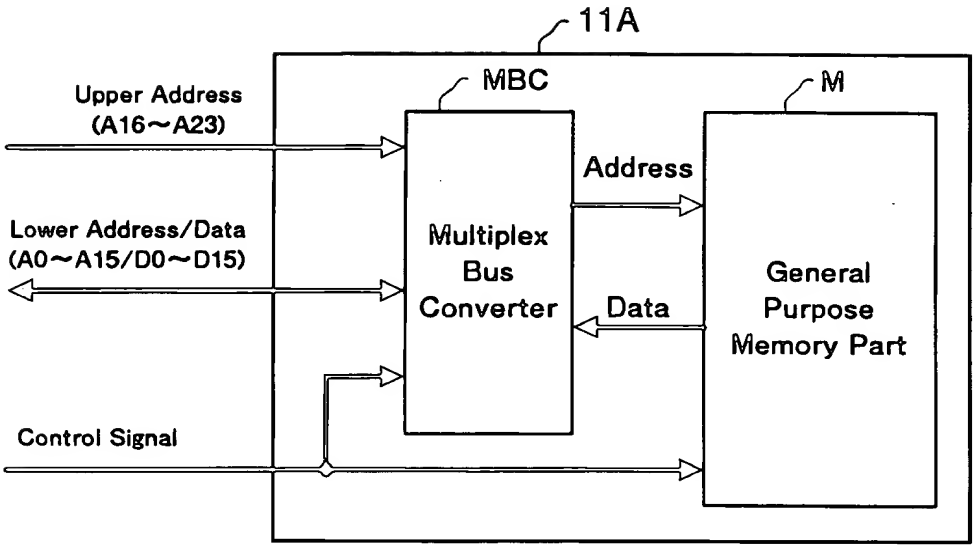


Fig. 21A

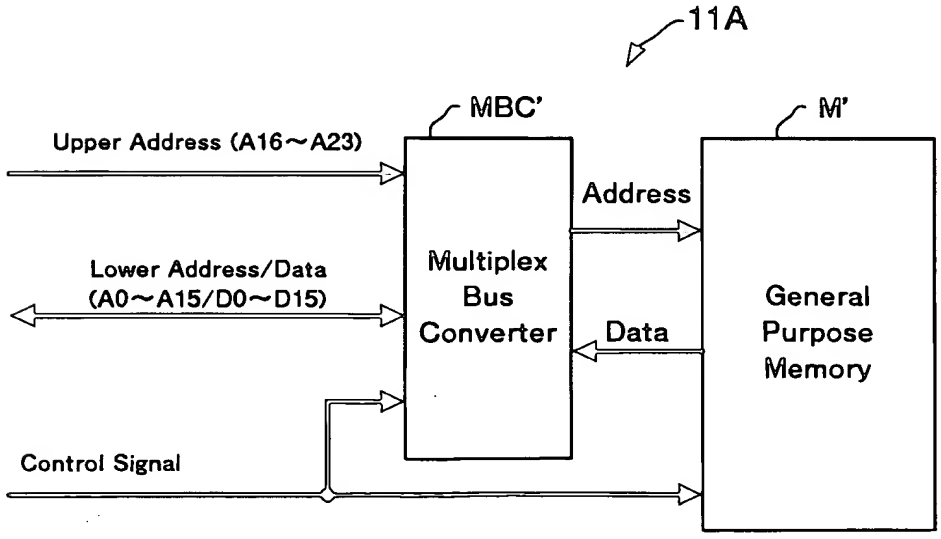


Fig. 21B

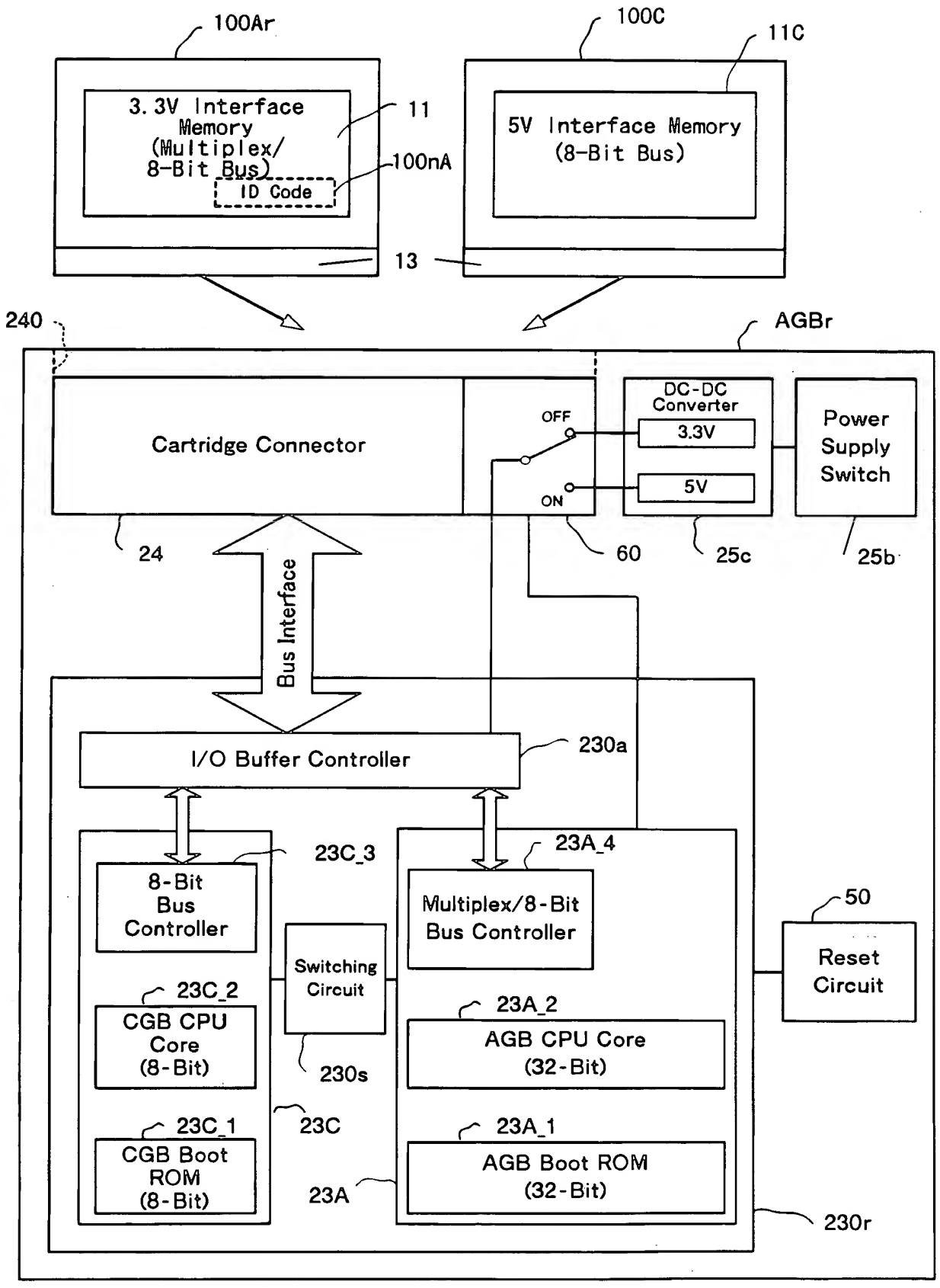

100Ar
100C
11C
3.3V Interface Memory (Multiplex/ 8-Bit Bus)
11
100nA
ID Code
5V Interface Memory (8-Bit Bus)
13
240
AGBr
Cartridge Connector
OFF
ON
DC-DC Converter
3.3V
5V
Power Supply Switch
24
60
25c
25b
Bus Interface
I/O Buffer Controller
230a
23C_3
8-Bit Bus Controller
23A_4
Multiplex/8-Bit Bus Controller
50
Reset Circuit
Switching Circuit
23C_2
CGB CPU Core (8-Bit)
23A_2
AGB CPU Core (32-Bit)
230s
23C
23C_1
CGB Boot ROM (8-Bit)
23A_1
AGB Boot ROM (32-Bit)
23A
230r

Fig. 22

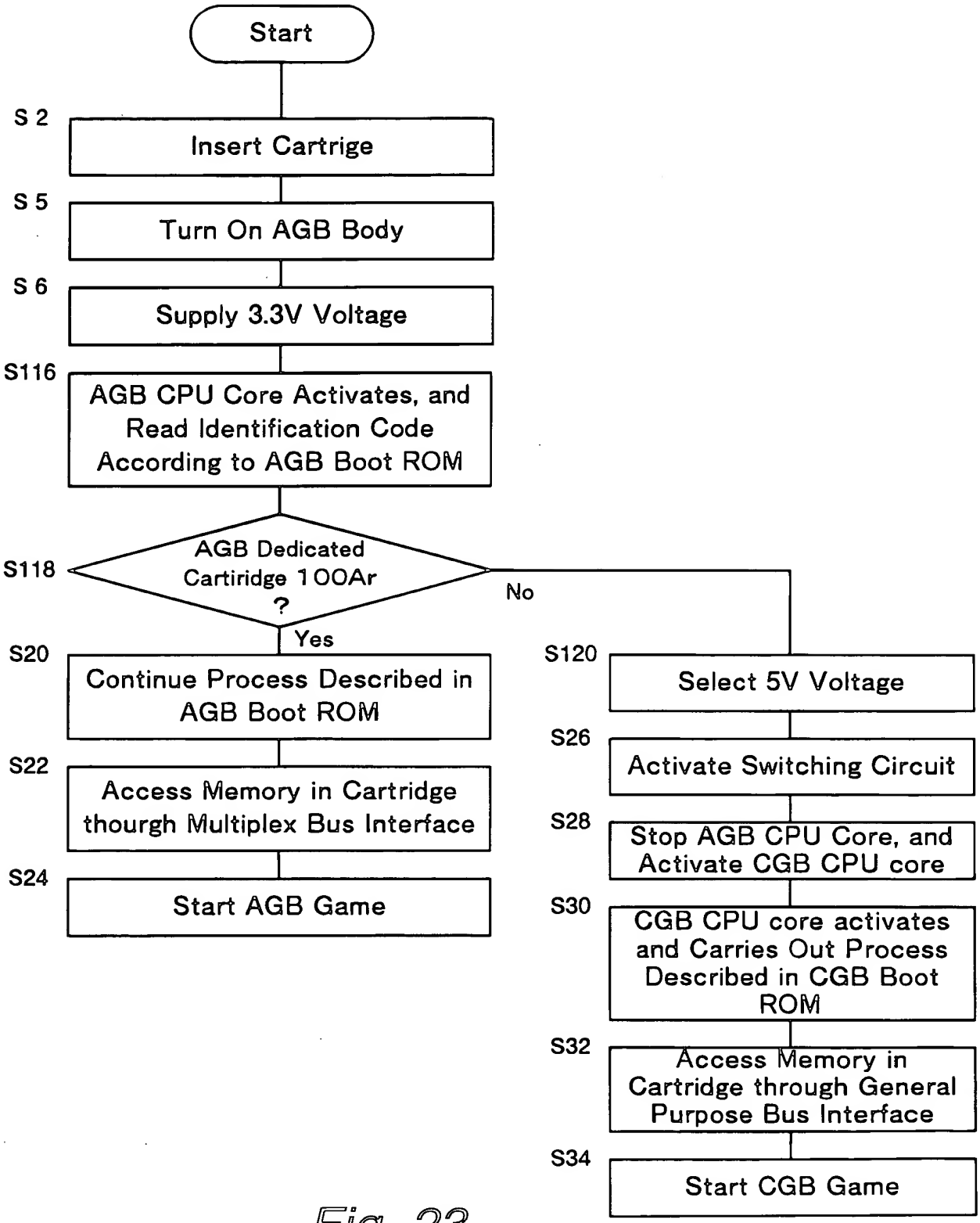

Start
S 2
Insert Cartrige
S 5
Turn On AGB Body
S 6
Supply 3.3V Voltage
S116
AGB CPU Core Activates, and Read Identification Code According to AGB Boot ROM
S118
AGB Dedicated Cartiridge 100Ar ?
No
Yes
S20
Continue Process Described in AGB Boot ROM
S22
Access Memory in Cartridge thourgh Multiplex Bus Interface
S24
Start AGB Game
S120
Select 5V Voltage
S26
Activate Switching Circuit
S28
Stop AGB CPU Core, and Activate CGB CPU core
S30
CGB CPU core activates and Carries Out Process Described in CGB Boot ROM
S32
Access Memory in Cartridge through General Purpose Bus Interface
S34
Start CGB Game

Fig. 23

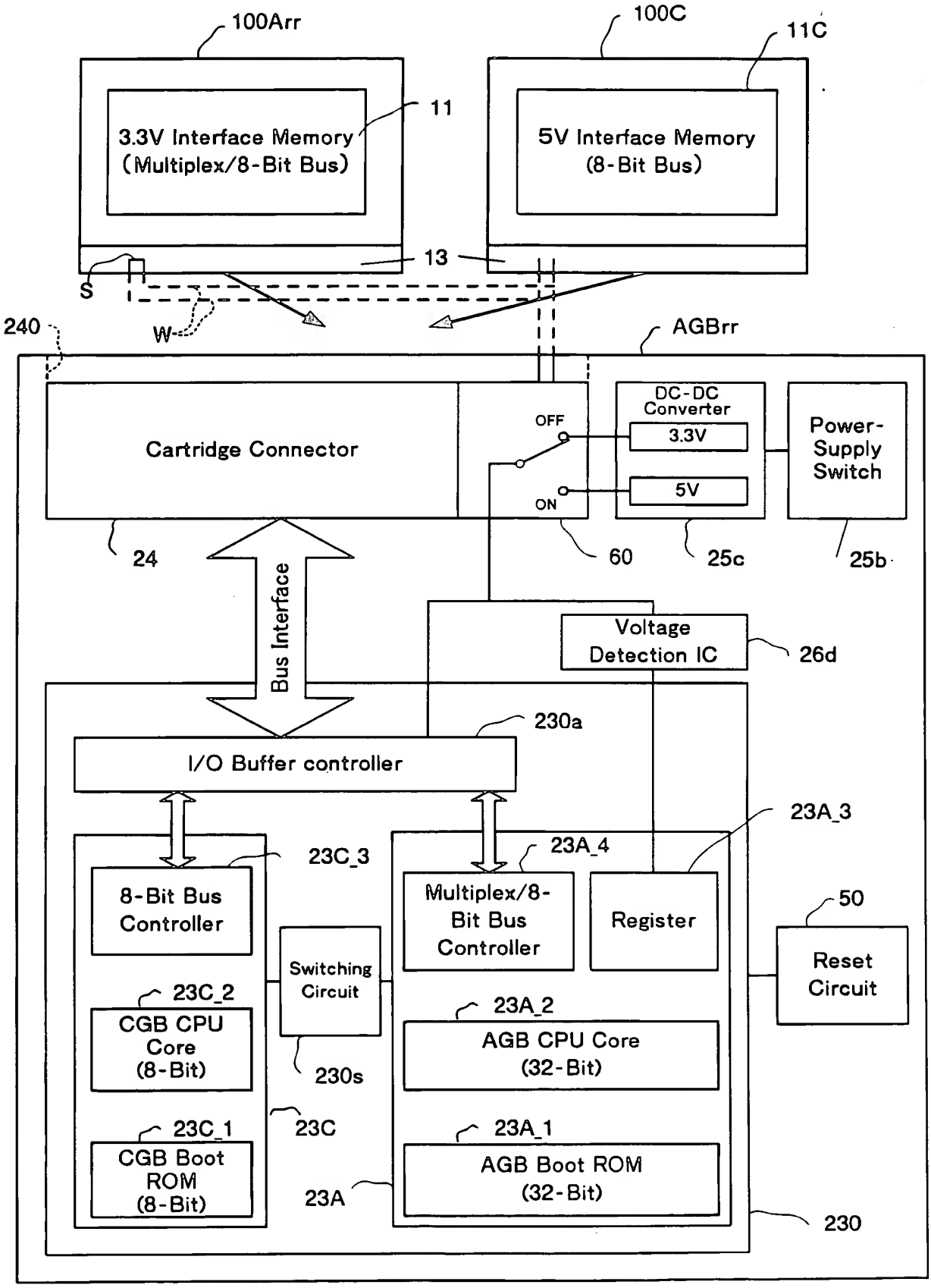

100Arr
100C
11C
3.3V Interface Memory
(Multiplex/8-Bit Bus)
11
5V Interface Memory
(8-Bit Bus)
13
S
W
240
AGBrr
Cartridge Connector
OFF
ON
DC-DC
Converter
3.3V
5V
Power-
Supply
Switch
24
Bus Interface
60
25c
25b
Voltage
Detection IC
26d
230a
I/O Buffer controller
23A_3
23C_3
23A_4
8-Bit Bus
Controller
Multiplex/8-
Bit Bus
Controller
Register
50
Switching
Circuit
Reset
Circuit
23C_2
CGB CPU
Core
(8-Bit)
23A_2
AGB CPU Core
(32-Bit)
230s
23C_1
23C
23A_1
CGB Boot
ROM
(8-Bit)
AGB Boot ROM
(32-Bit)
23A
230

Fig. 24

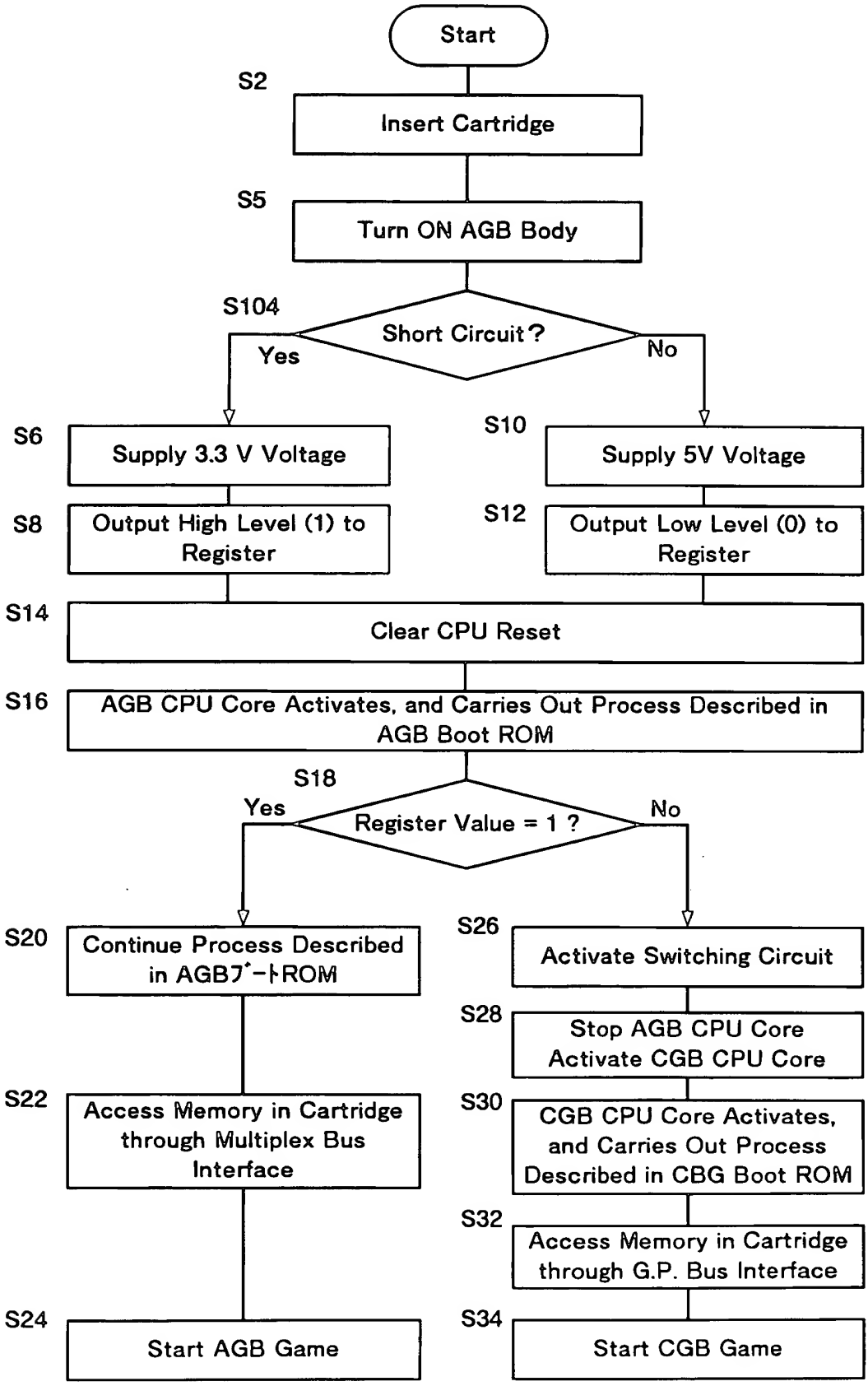

Start
S2
Insert Cartridge
S5
Turn ON AGB Body
S104
Short Circuit?
Yes
No
S6
Supply 3.3 V Voltage
S8
Output High Level (1) to Register
S10
Supply 5V Voltage
S12
Output Low Level (0) to Register
S14
Clear CPU Reset
S16
AGB CPU Core Activates, and Carries Out Process Described in AGB Boot ROM
S18
Yes
Register Value = 1 ?
No
S20
Continue Process Described in AGBﾌﾟﾘﾝﾄROM
S22
Access Memory in Cartridge through Multiplex Bus Interface
S24
Start AGB Game
S26
Activate Switching Circuit
S28
Stop AGB CPU Core Activate CGB CPU Core
S30
CGB CPU Core Activates, and Carries Out Process Described in CBG Boot ROM
S32
Access Memory in Cartridge through G.P. Bus Interface
S34
Start CGB Game

Fig. 25

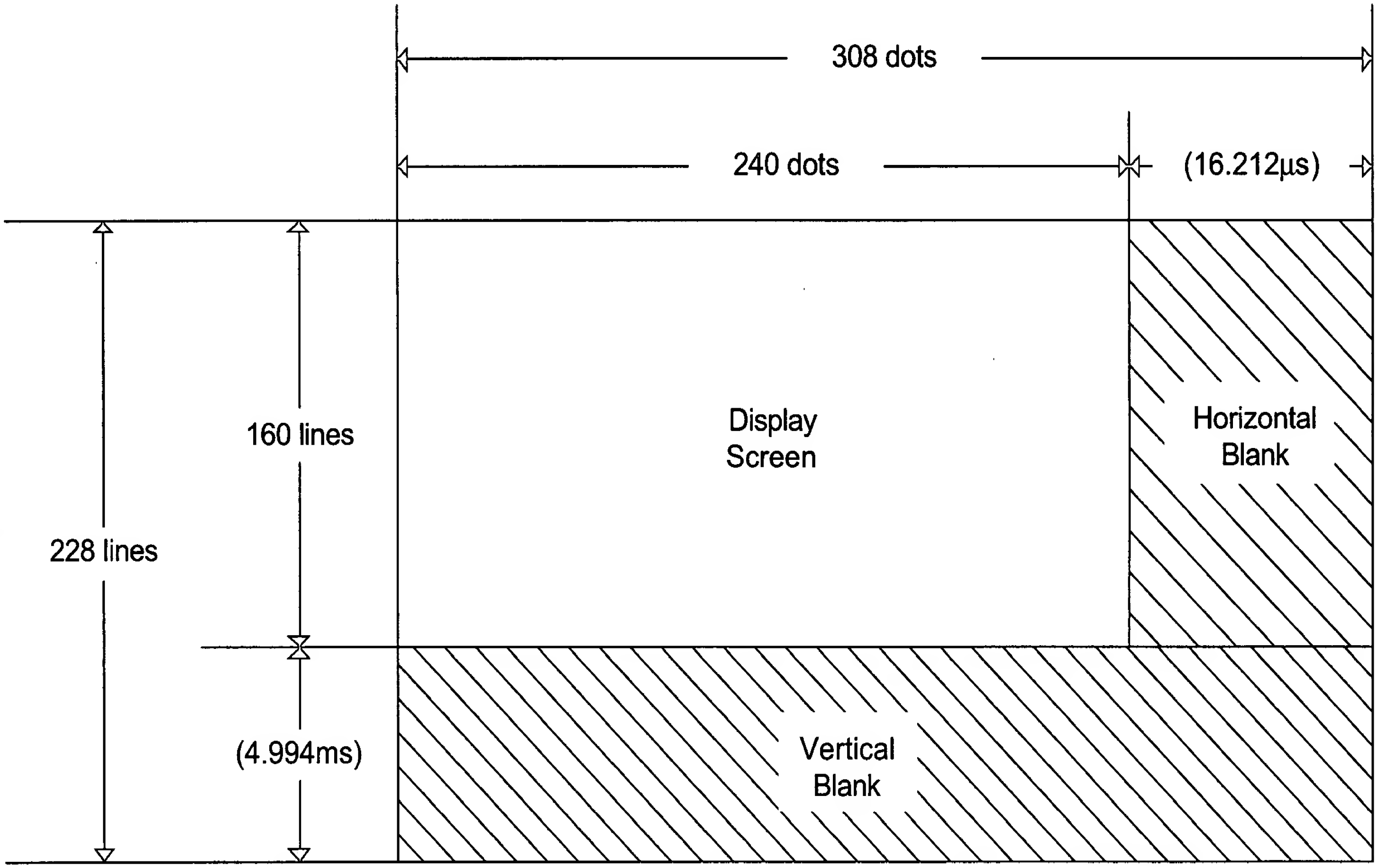

308 dots
240 dots
(16.212µs)
160 lines
228 lines
(4.994ms)
Display
Screen
Horizontal
Blank
Vertical
Blank

Fig. 26

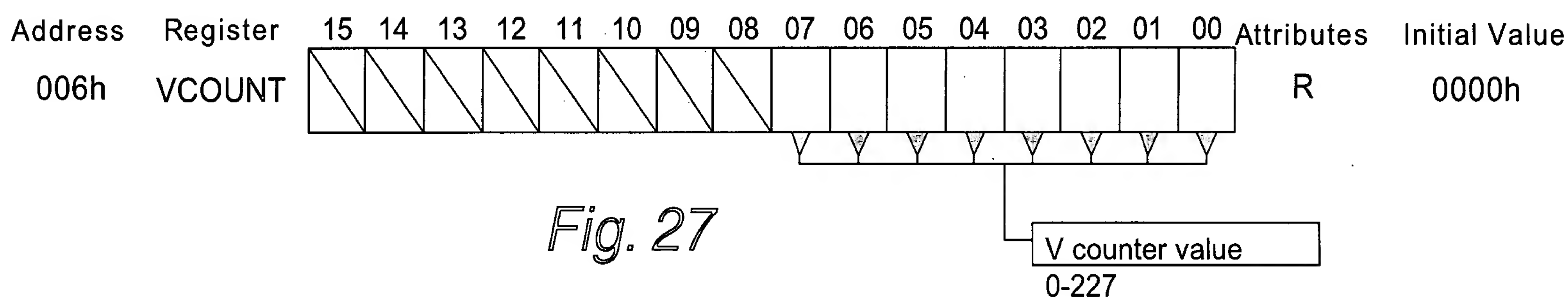

Address
Register
15
14
13
12
11
10
09
08
07
06
05
04
03
02
01
00
Attributes
Initial Value
006h
VCOUNT
R
0000h
V counter value
0-227

Fig. 27

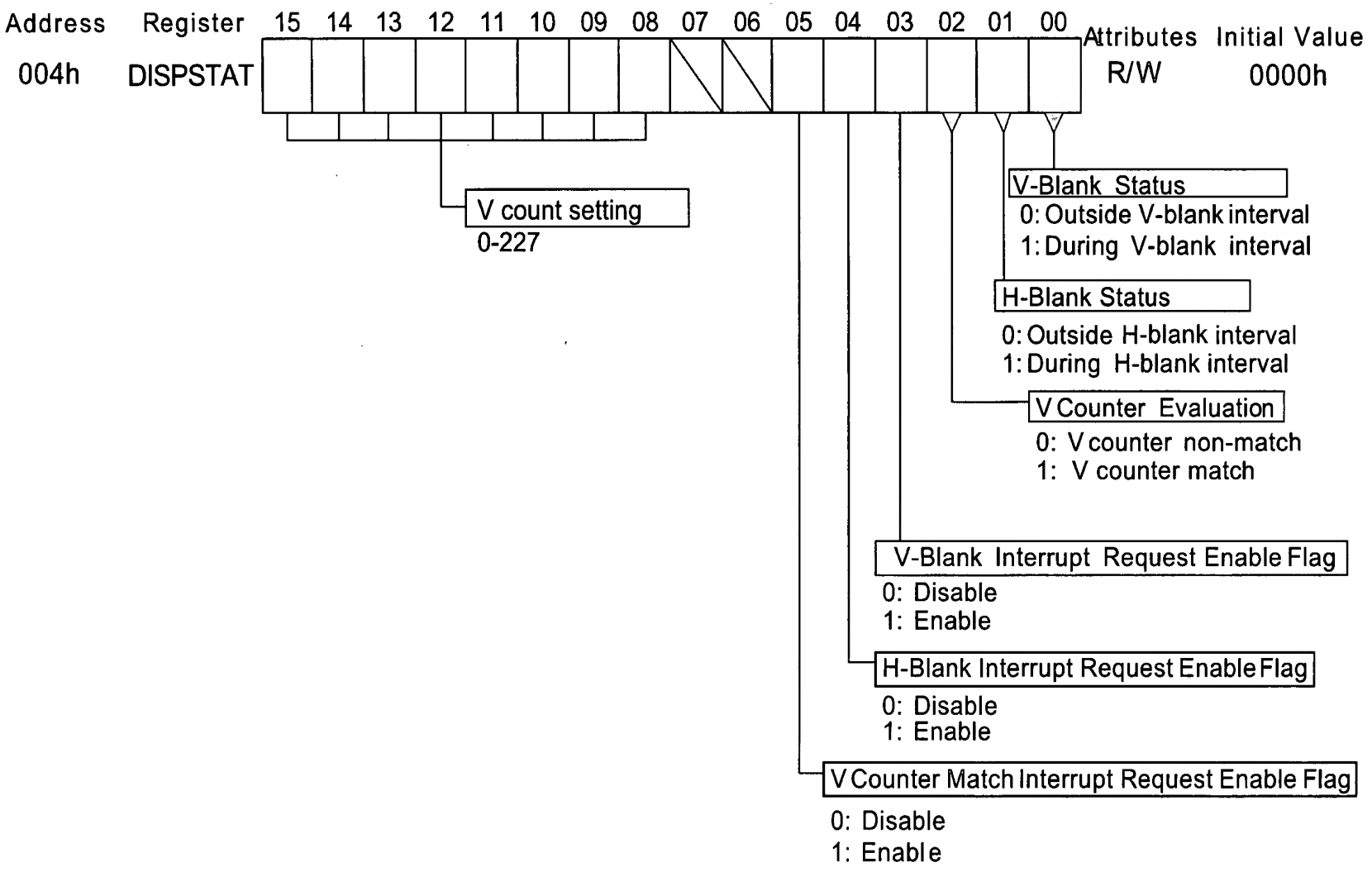

Address
Register
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Attributes
Initial Value
004h
DISPSTAT
R/W
0000h
V count setting
0-227
V-Blank Status
0: Outside V-blank interval
1: During V-blank interval
H-Blank Status
0: Outside H-blank interval
1: During H-blank interval
V Counter Evaluation
0: V counter non-match
1: V counter match
V-Blank Interrupt Request Enable Flag
0: Disable
1: Enable
H-Blank Interrupt Request Enable Flag
0: Disable
1: Enable
V Counter Match Interrupt Request Enable Flag
0: Disable
1: Enable

Fig. 28

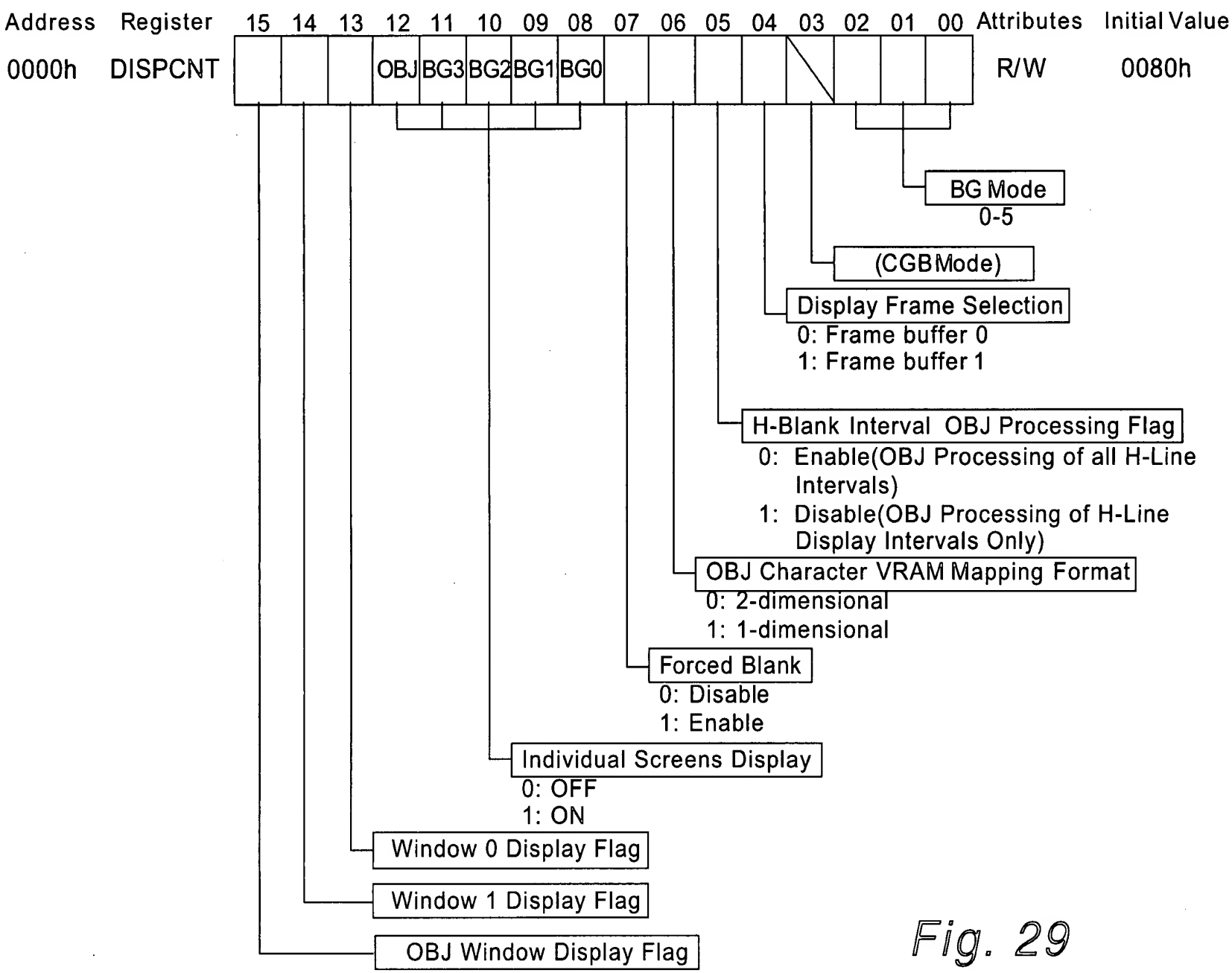


Fig. 29

Fig. 30A

BG Mode	Character Format BG Screen			Number of Characters Specifiable	Number of Colors/ Palettes	Features					
	Rotation/ scaling	No. of Screens	Size			*1	*2	*3	*4	*5	*6
0	No	4	256 x 256 to 512 x 512	1024	16/16 256/1	O	O	O	O	O	O
1	No	2	256 x 256 to 512 x 512	1024	16/16 256/1	O	O	O	O	O	O
	Yes	1	128 x 128 to 1024 x 1024	256	256/1	O	X	O	O	O	O
2	Yes	2	128 x 128 to 1024 x 1024	256	256/1	O	X	O	O	O	O

*1 HV Scroll (individual screens)
*2 HV Flip (individual characters)
*3 Mosaic (16 levels)
*4 Semi-transparent (16 levels)
*5 Fade-in/Fade-out
*6 Screen priority specification (2 bits)

Fig. 30B

BG Mode	Bitmap Format BG Screen			Frame Memory	No. of Colors	Features					
	Rotation/ Scaling	No. of Screens	Size			*1	*2	*3	*4	*5	*6
3	Yes	1	240 x 160	1	32,768	O	X	O	O	O	O
4	Yes	1	240 x160	2	256	O	X	O	O	O	O
5	Yes	1	160 x 128	2	32,768	O	X	O	O	O	O

*1 HV Scroll (individual screens)
*2 HV Flip (individual characters)
*3 Mosaic (16 levels)
*4 Semi-transparent (16 levels)
*5 Fade-in/Fade-out
*6 Screen priority specification (2 bits)

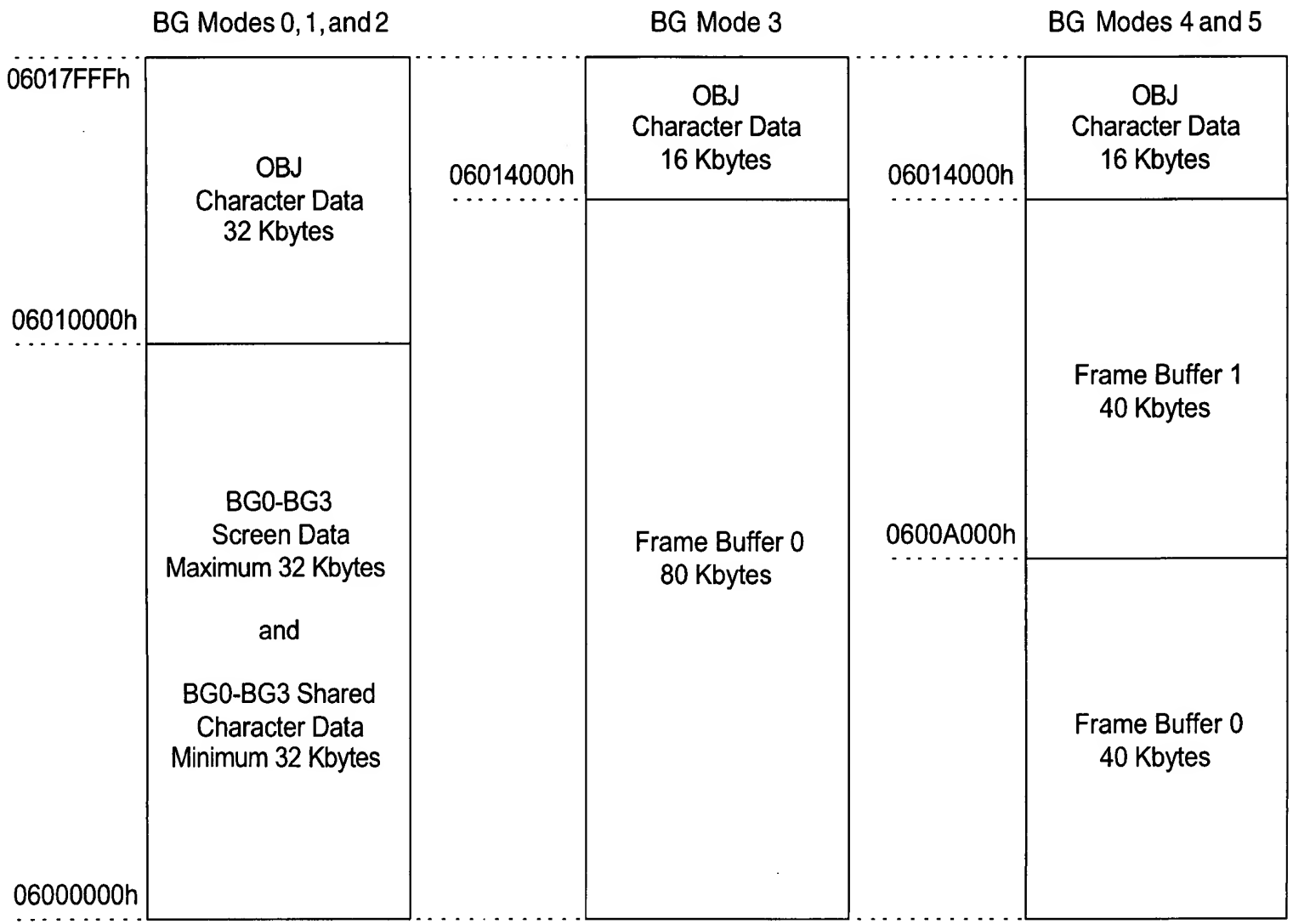


Fig. 31

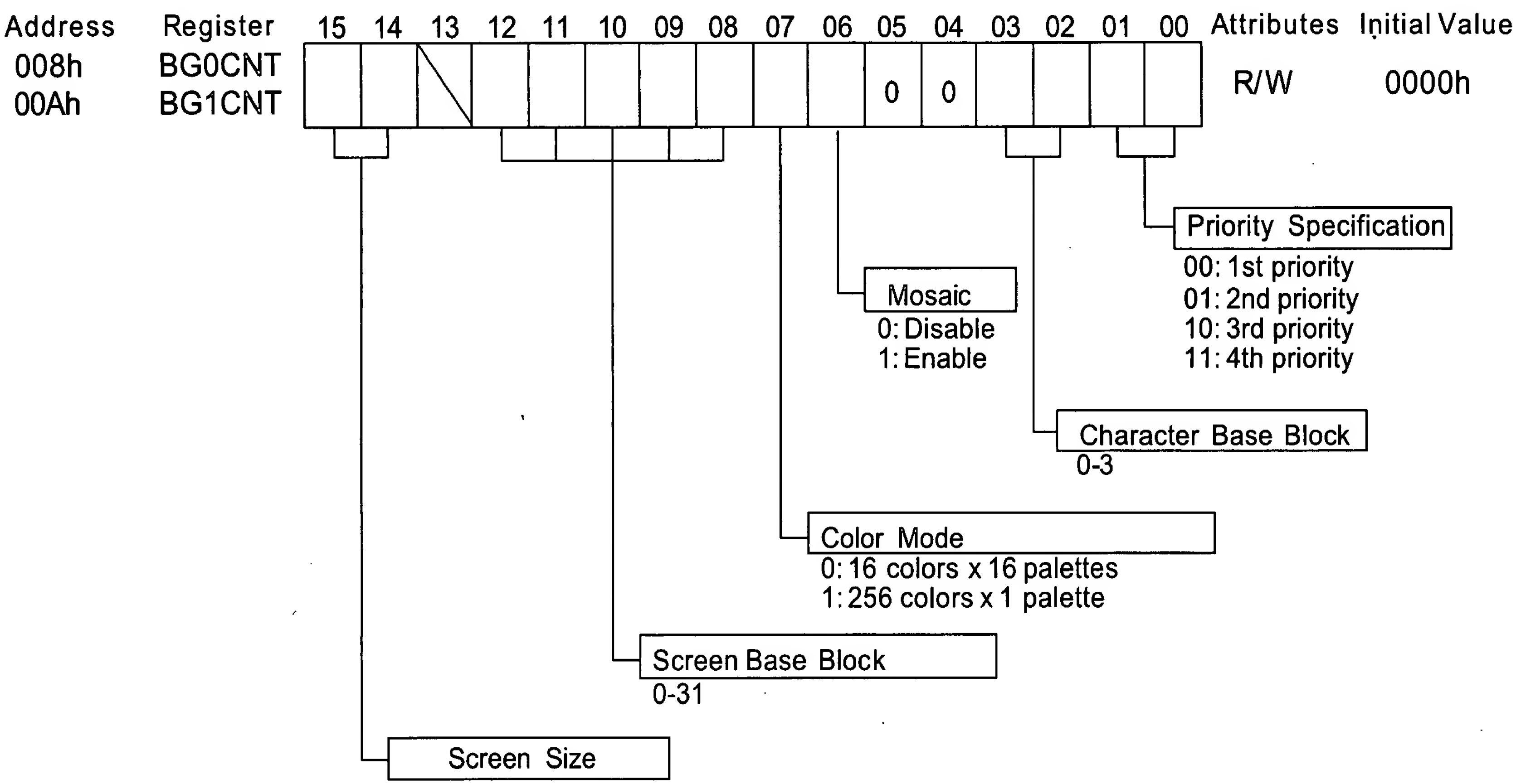

Address
008h
00Ah
Register
BG0CNT
BG1CNT
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
0
0
Attributes
R/W
Initial Value
0000h
Priority Specification
00: 1st priority
01: 2nd priority
10: 3rd priority
11: 4th priority
Mosaic
0: Disable
1: Enable
Character Base Block
0-3
Color Mode
0: 16 colors x 16 palettes
1: 256 colors x 1 palette
Screen Base Block
0-31
Screen Size

Fig. 32A

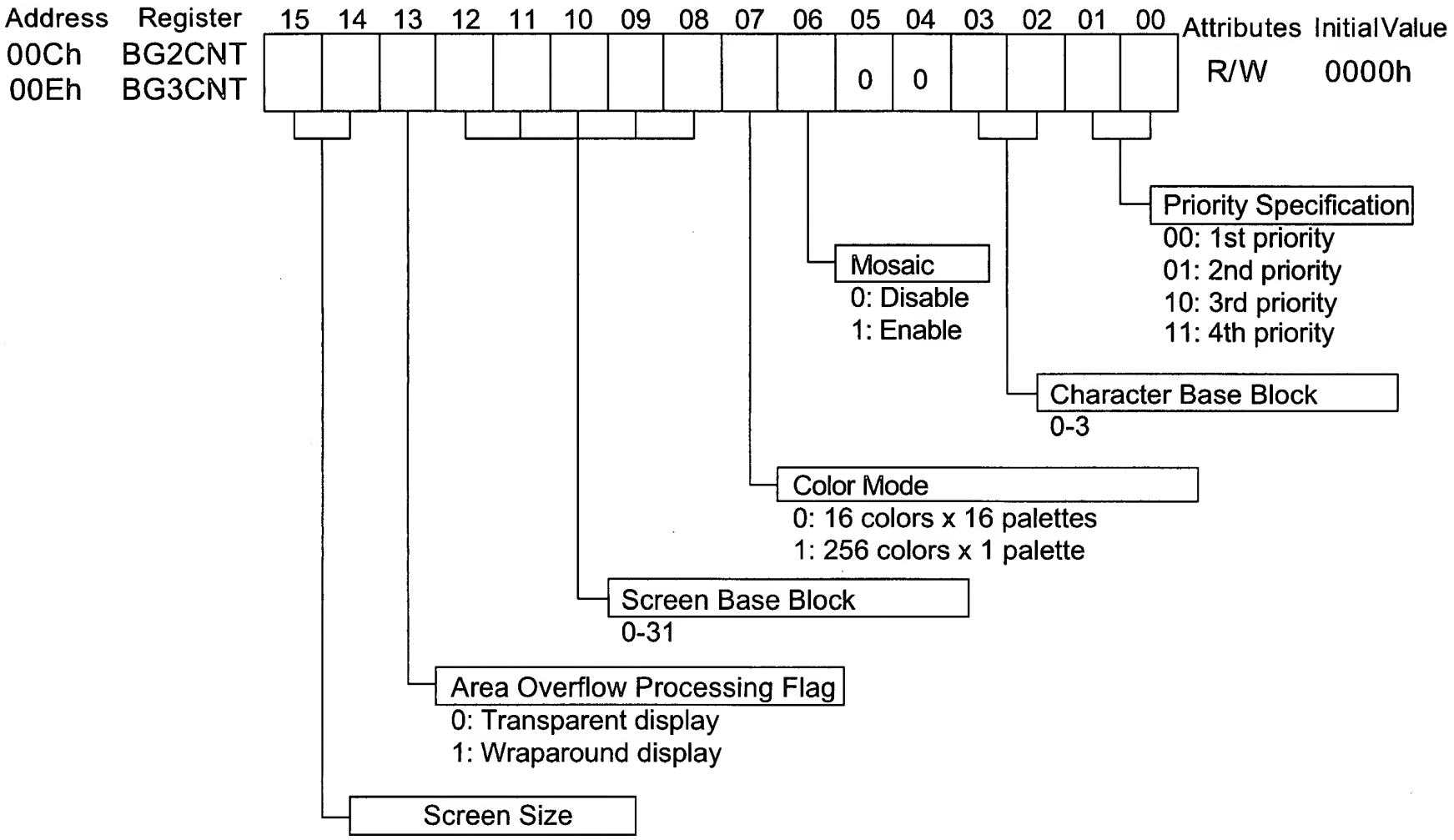


Fig. 32B

[d15,d14]=[0,0] Virtual screen size:256 x 256

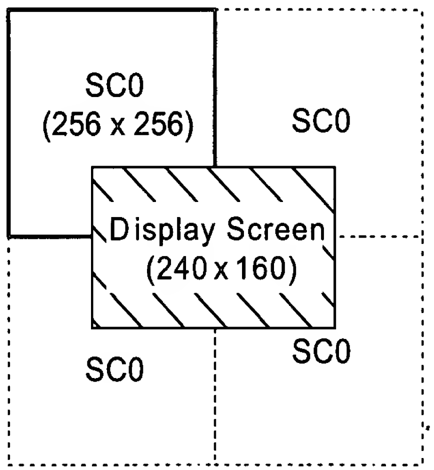


Fig. 33A

[d15,d14]=[0,1] Virtual Screen size: 512 x 256

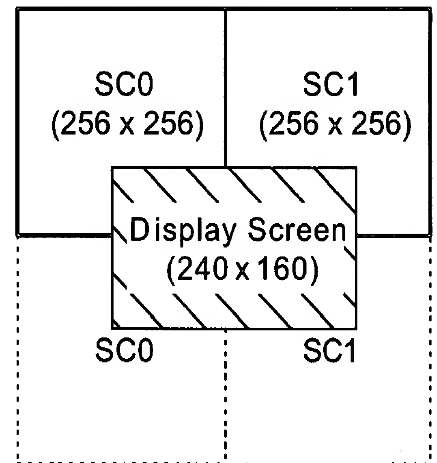


Fig. 33B

[d15,d14]=[1,0] Virtual screen size: 256 x 512

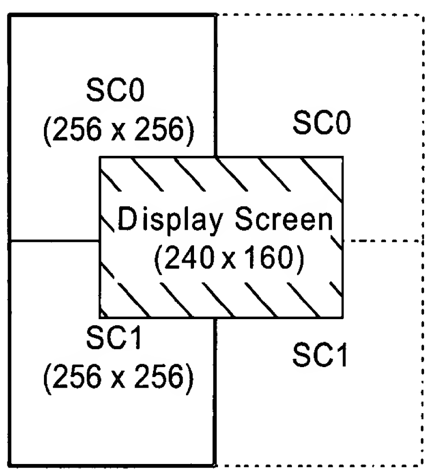


Fig. 33C

[d15,d14]=[1,1] Virtual screen size: 512 x 512

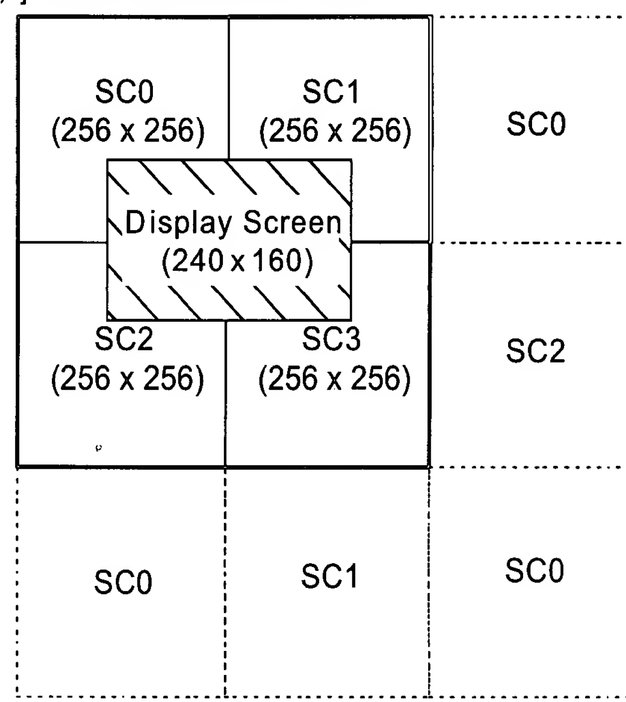


Fig. 33D

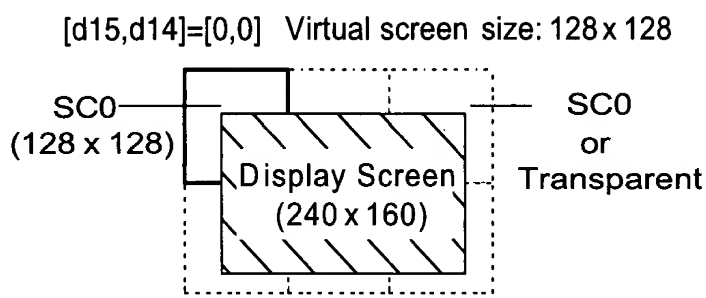


Fig. 34A

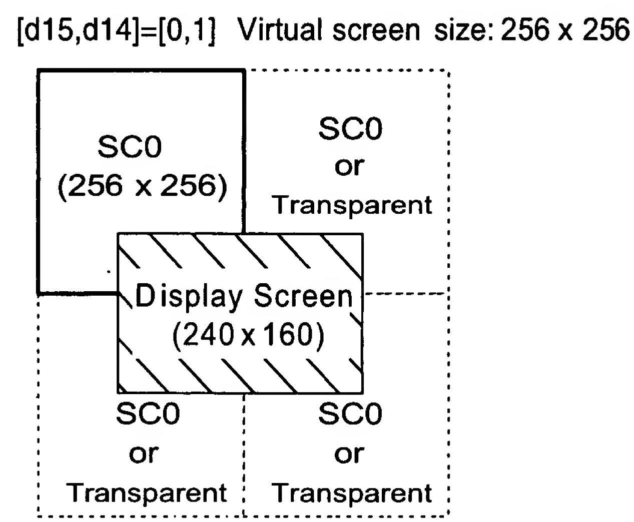


Fig. 34B

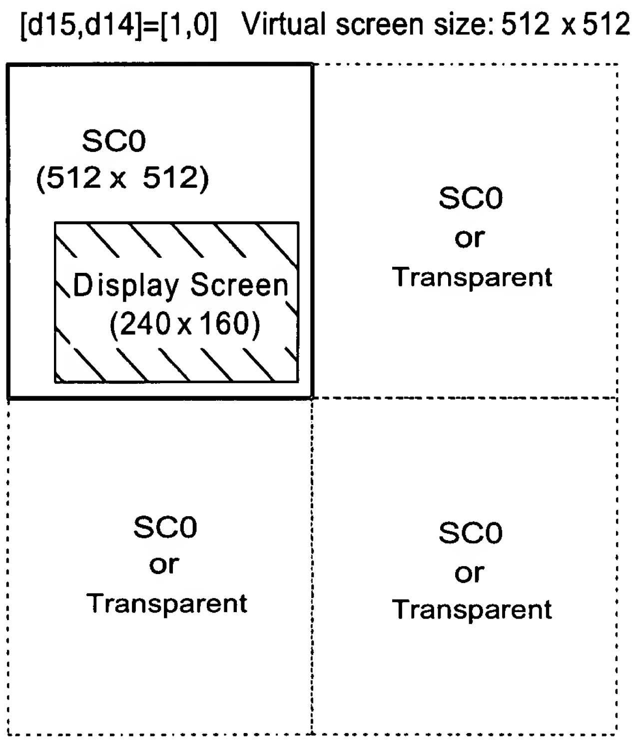


Fig. 34C

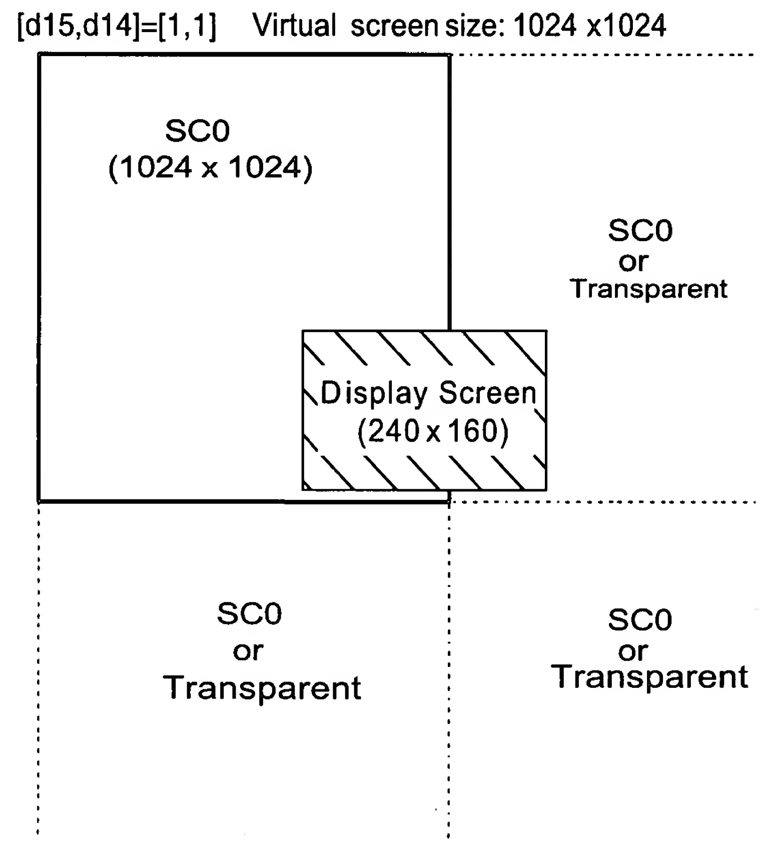


Fig. 34D

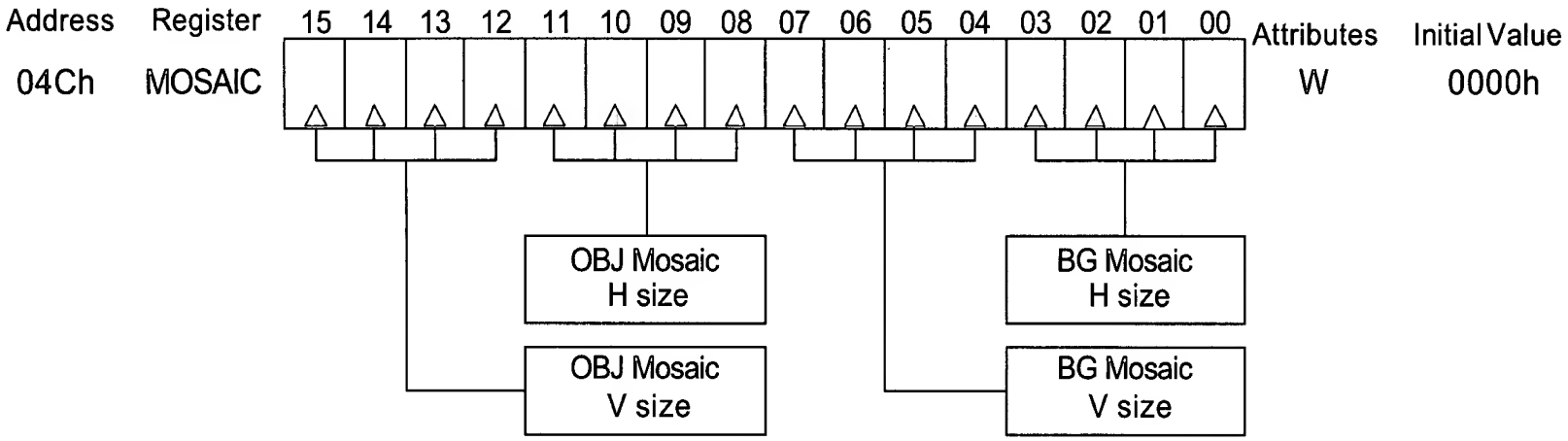


Fig. 35

Normal Display

00	01	02	03	04	05	06	07	08	09
10	11	12	13	14	15	16	17	18	19
20	21	22	23	24	25	26	27	28	29
30	31	32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47	48	49
50	51	52	53	54	55	56	57	58	59
60	61	62	63	64	65	66	67	68	69
70	71	72	73	74	75	76	77	78	79

Fig. 36A

Mosaic H size: 1
V size: 1

00	00	02	04	06	08
00	00				
20		22	24	26	28
40		42	44	46	48
60		62	64	66	68

Fig. 36B

Mosaic H size: 3
V size: 5

00	00	00	00	04	08
00	00	00	00		
00	00	00	00		
00	00	00	00		
00	00	00	00		
00	00	00	00		
60				64	68

Fig. 36C

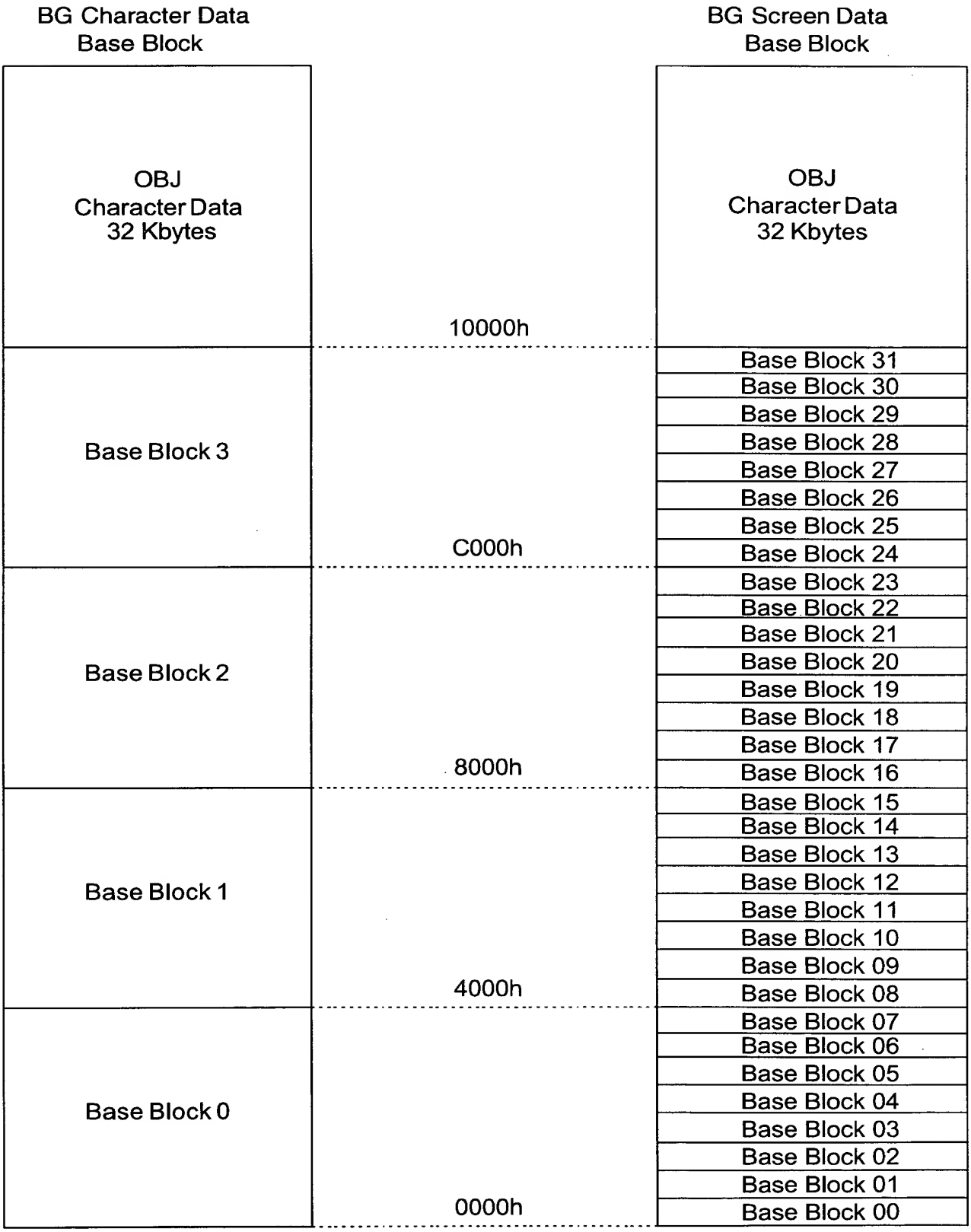

BG Character Data
Base Block
BG Screen Data
Base Block
OBJ
Character Data
32 Kbytes
10000h
Base Block 3
C000h
Base Block 2
8000h
Base Block 1
4000h
Base Block 0
0000h
Base Block 31
Base Block 30
Base Block 29
Base Block 28
Base Block 27
Base Block 26
Base Block 25
Base Block 24
Base Block 23
Base Block 22
Base Block 21
Base Block 20
Base Block 19
Base Block 18
Base Block 17
Base Block 16
Base Block 15
Base Block 14
Base Block 13
Base Block 12
Base Block 11
Base Block 10
Base Block 09
Base Block 08
Base Block 07
Base Block 06
Base Block 05
Base Block 04
Base Block 03
Base Block 02
Base Block 01
Base Block 00

Fig. 37

16 Colors x 16 Palettes

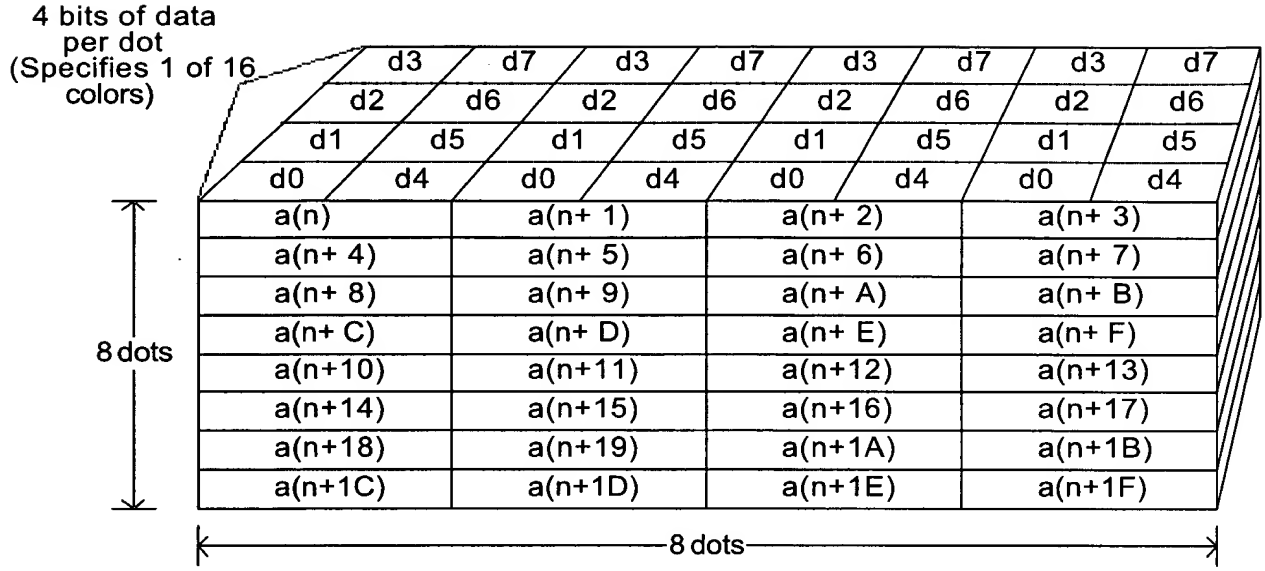


Fig. 38A

256 Colors x 1 Palettes

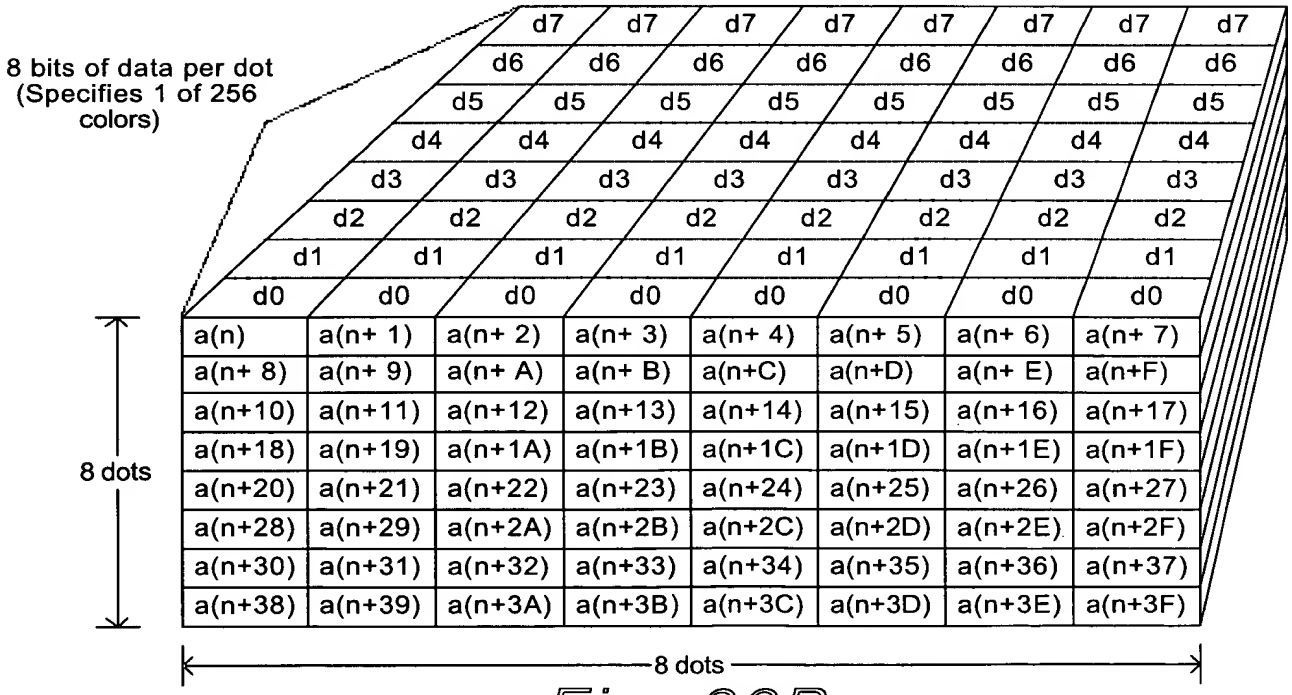


Fig. 38B

Text BG screen data format

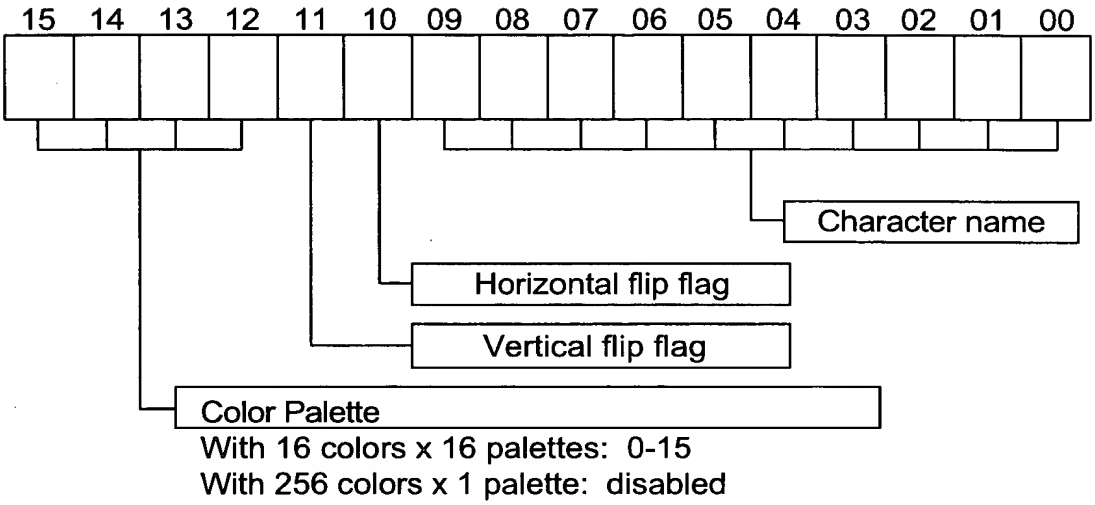


Fig. 39A

Rotation/scaling BG screen data format

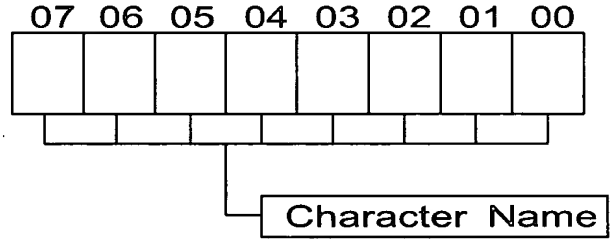


Fig. 39B

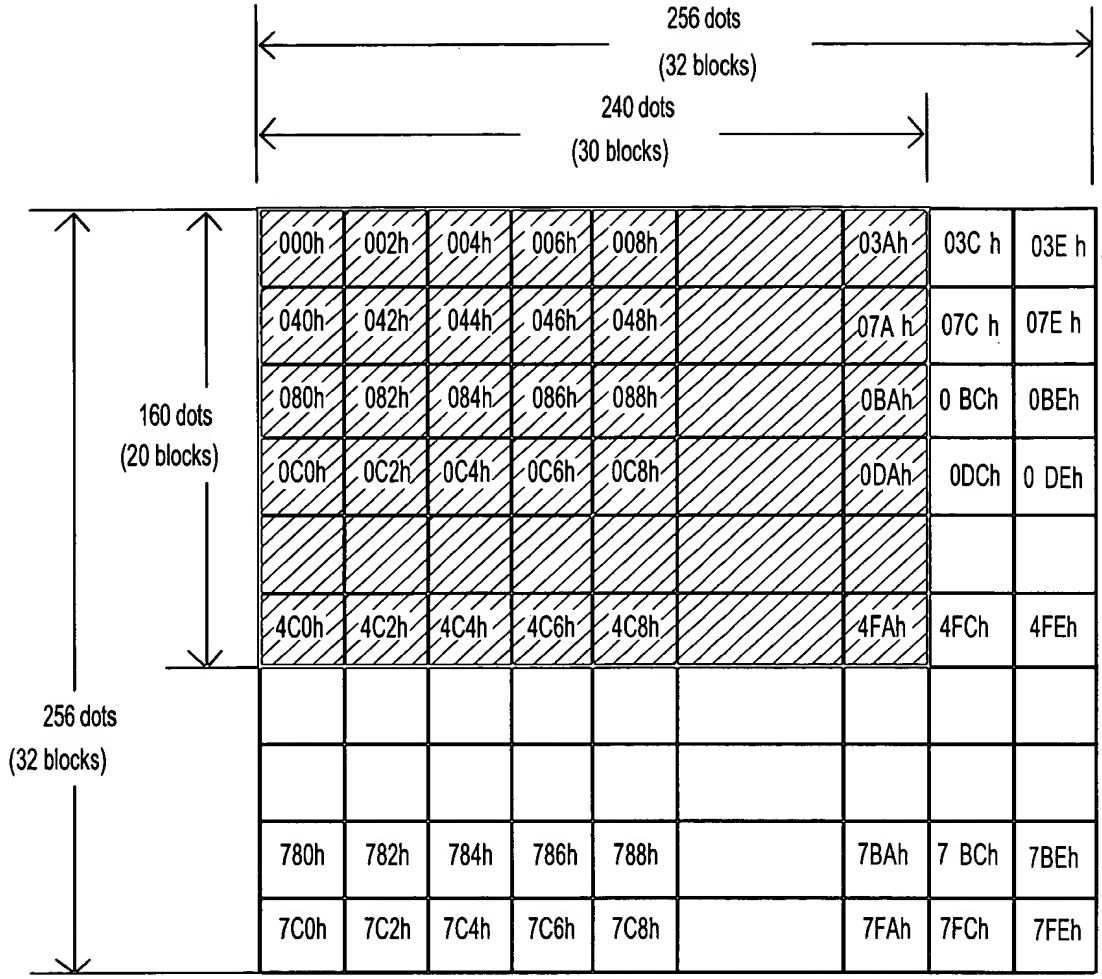


Fig. 40A

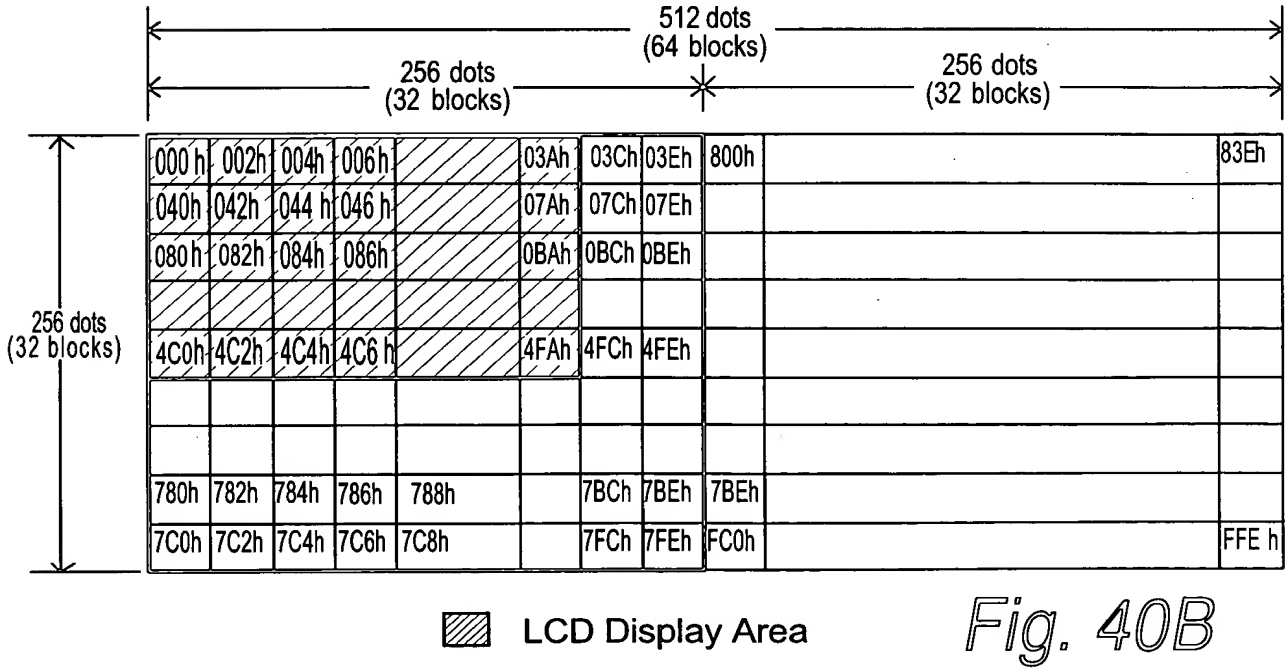


Fig. 40B

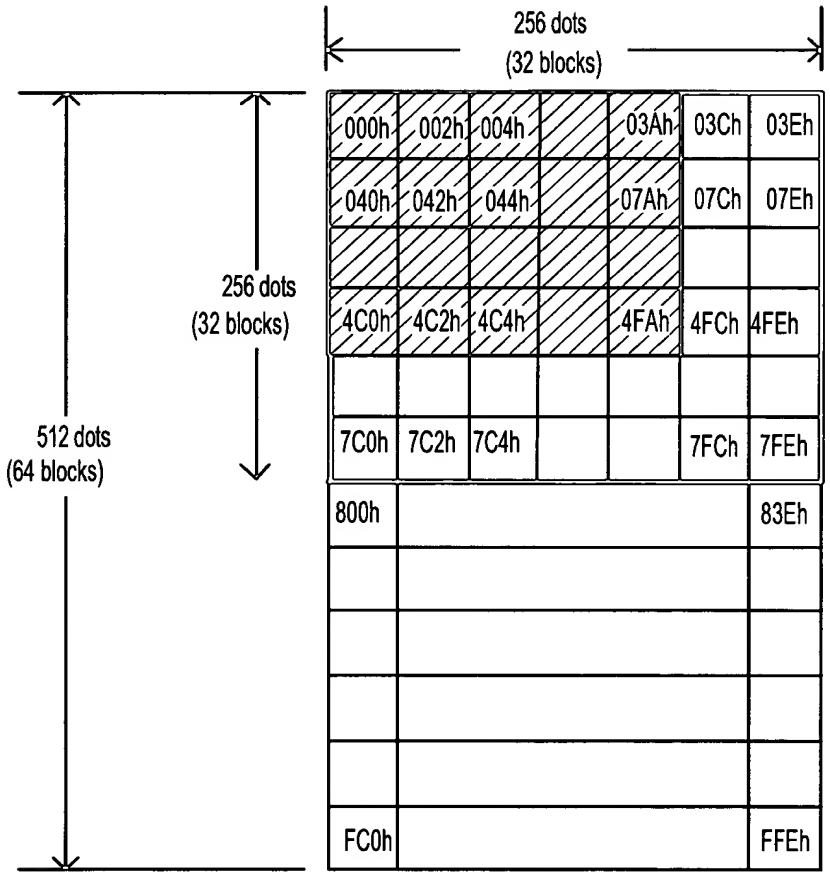

256 dots
(32 blocks)
256 dots
(32 blocks)
512 dots
(64 blocks)
000h
002h
004h
03Ah
03Ch
03Eh
040h
042h
044h
07Ah
07Ch
07Eh
4C0h
4C2h
4C4h
4FAh
4FCh
4FEh
7C0h
7C2h
7C4h
7FCh
7FEh
800h
83Eh
FC0h
FFEh
LCD Display Area

Fig. 40C

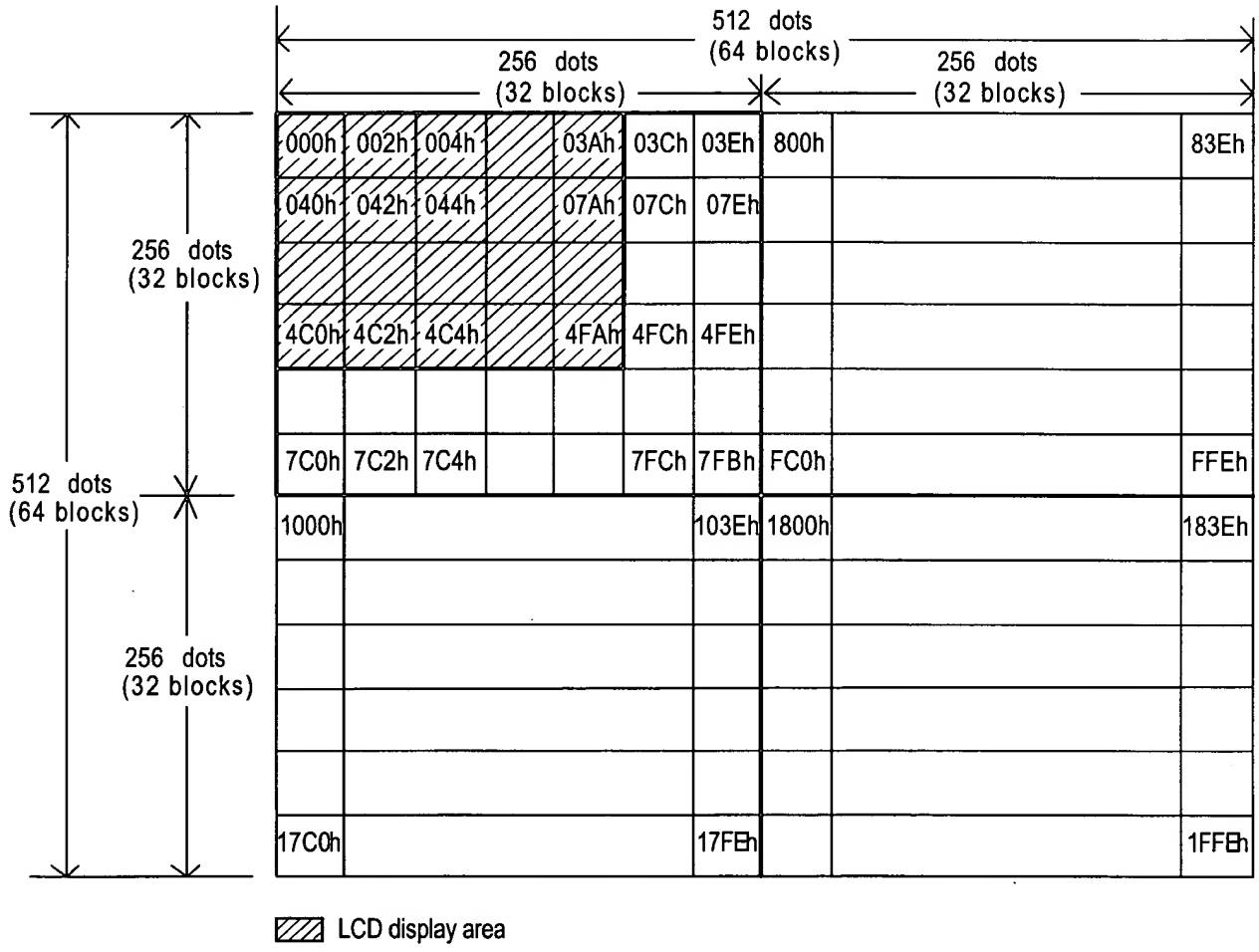

512 dots
(64 blocks)
256 dots
(32 blocks)
256 dots
(32 blocks)
256 dots
(32 blocks)
512 dots
(64 blocks)
256 dots
(32 blocks)
000h
002h
004h
03Ah
03Ch
03Eh
800h
83Eh
040h
042h
044h
07Ah
07Ch
07Eh
4C0h
4C2h
4C4h
4FAh
4FCh
4FEh
7C0h
7C2h
7C4h
7FCh
7FBh
FC0h
FFEh
1000h
103Eh
1800h
183Eh
17C0h
17FEh
1FFEh
LCD display area

Fig.40D

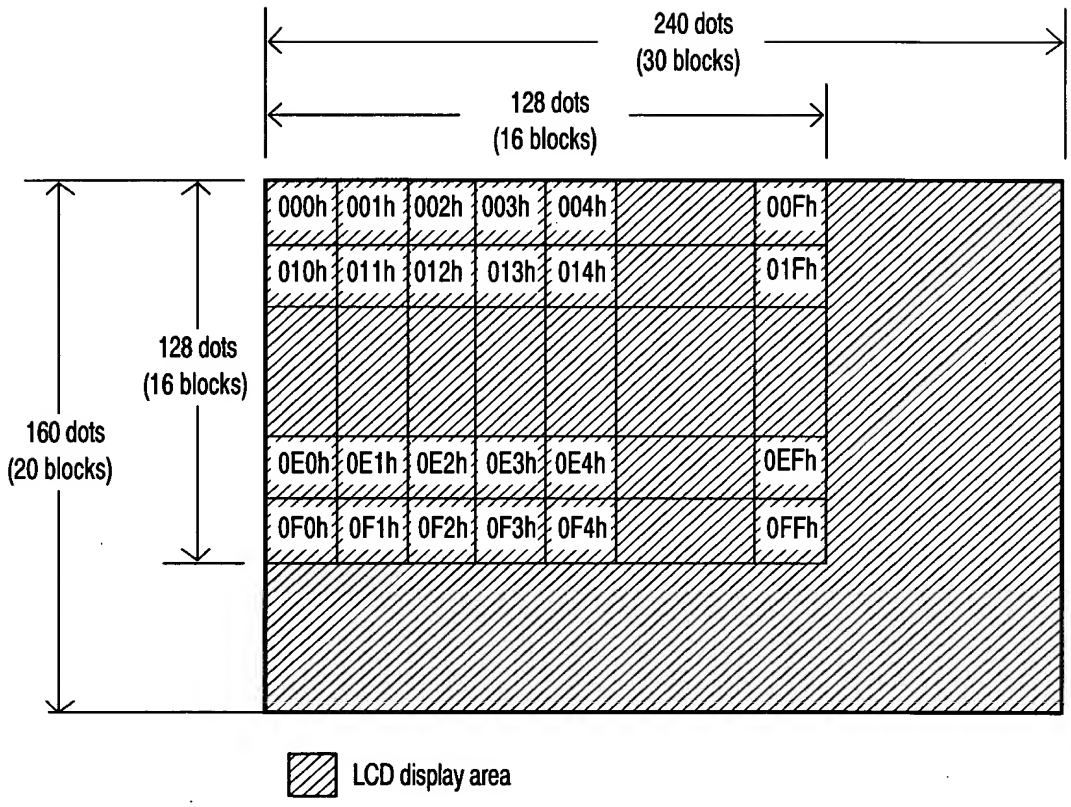

240 dots
(30 blocks)
128 dots
(16 blocks)
160 dots
(20 blocks)
128 dots
(16 blocks)
000h
001h
002h
003h
004h
00Fh
010h
011h
012h
013h
014h
01Fh
0E0h
0E1h
0E2h
0E3h
0E4h
0EFh
0F0h
0F1h
0F2h
0F3h
0F4h
0FFh
LCD display area

Fig.41A

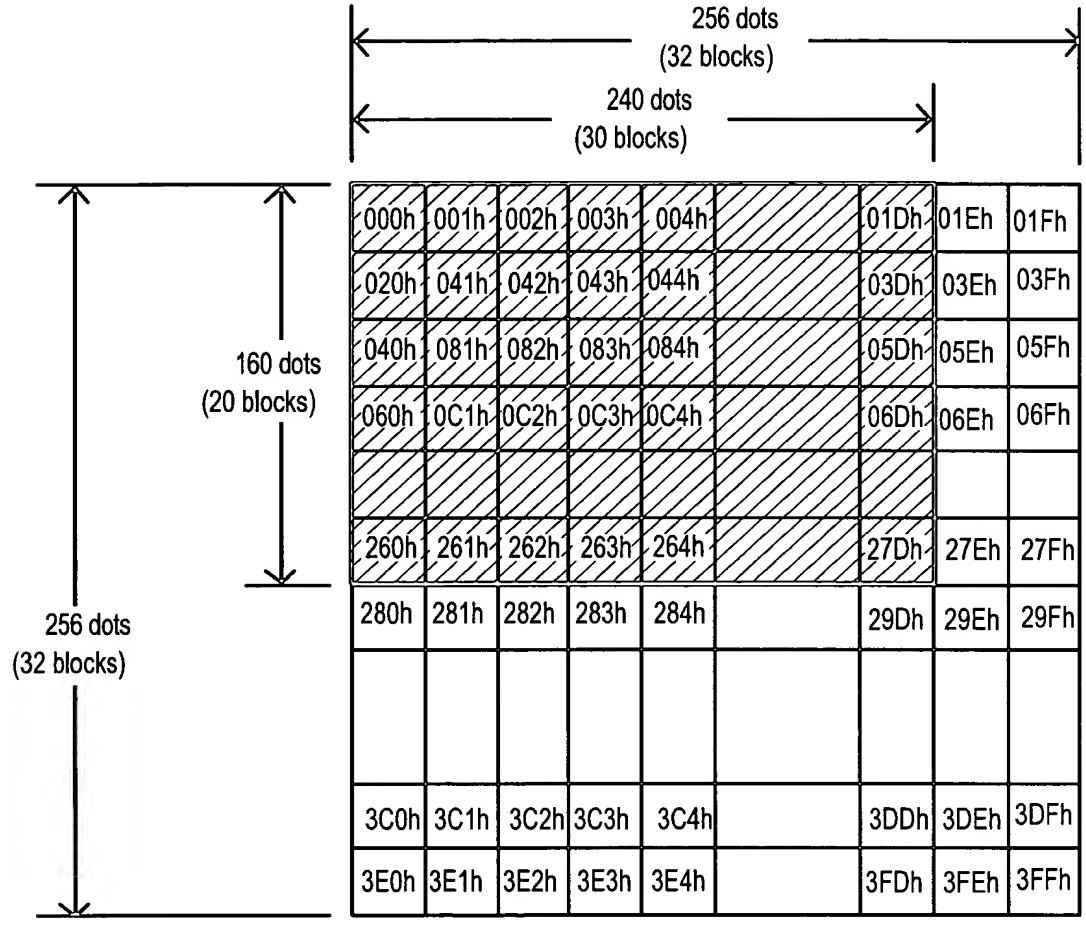

256 dots
(32 blocks)
240 dots
(30 blocks)
160 dots
(20 blocks)
256 dots
(32 blocks)
000h 001h 002h 003h 004h 01Dh 01Eh 01Fh
020h 041h 042h 043h 044h 03Dh 03Eh 03Fh
040h 081h 082h 083h 084h 05Dh 05Eh 05Fh
060h 0C1h 0C2h 0C3h 0C4h 06Dh 06Eh 06Fh
260h 261h 262h 263h 264h 27Dh 27Eh 27Fh
280h 281h 282h 283h 284h 29Dh 29Eh 29Fh
3C0h 3C1h 3C2h 3C3h 3C4h 3DDh 3DEh 3DFh
3E0h 3E1h 3E2h 3E3h 3E4h 3FDh 3FEh 3FFh
LCD Display Area

Fig. 41B

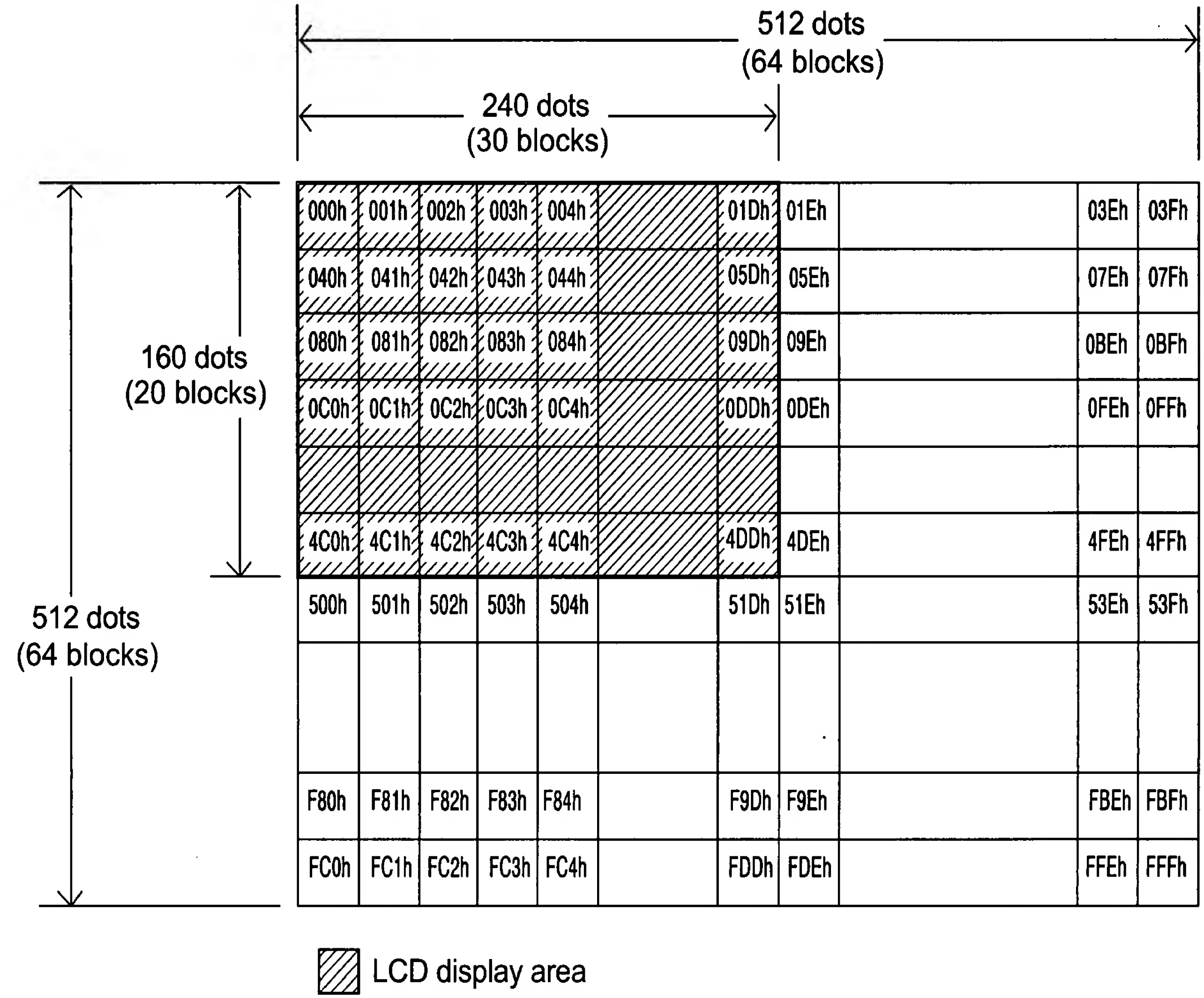

512 dots
(64 blocks)
240 dots
(30 blocks)
160 dots
(20 blocks)
512 dots
(64 blocks)
000h
001h
002h
003h
004h
01Dh
01Eh
03Eh
03Fh
040h
041h
042h
043h
044h
05Dh
05Eh
07Eh
07Fh
080h
081h
082h
083h
084h
09Dh
09Eh
0BEh
0BFh
0C0h
0C1h
0C2h
0C3h
0C4h
0DDh
0DEh
0FEh
0FFh
4C0h
4C1h
4C2h
4C3h
4C4h
4DDh
4DEh
4FEh
4FFh
500h
501h
502h
503h
504h
51Dh
51Eh
53Eh
53Fh
F80h
F81h
F82h
F83h
F84h
F9Dh
F9Eh
FBEh
FBFh
FC0h
FC1h
FC2h
FC3h
FC4h
FDDh
FDEh
FFEh
FFFh
LCD display area

Fig.41C

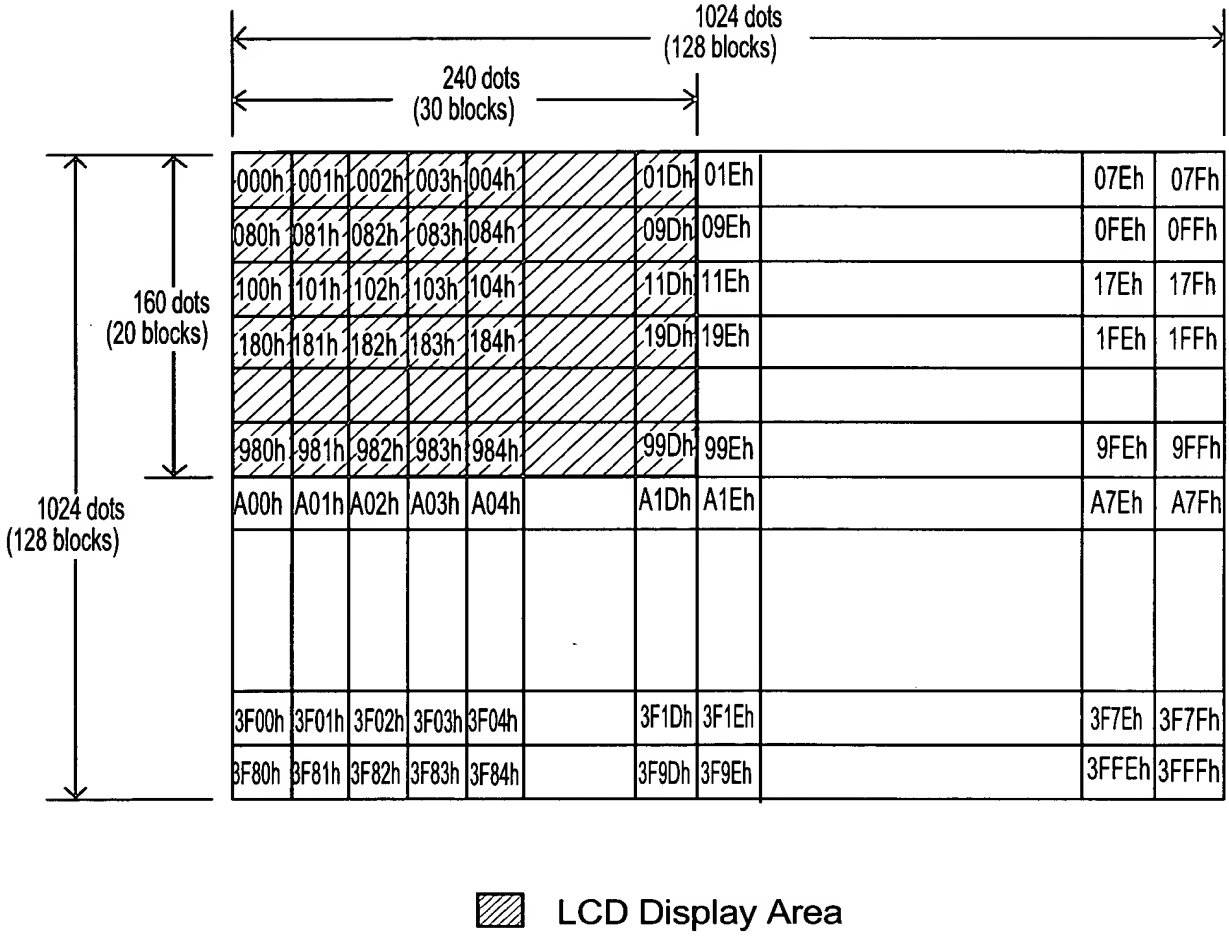
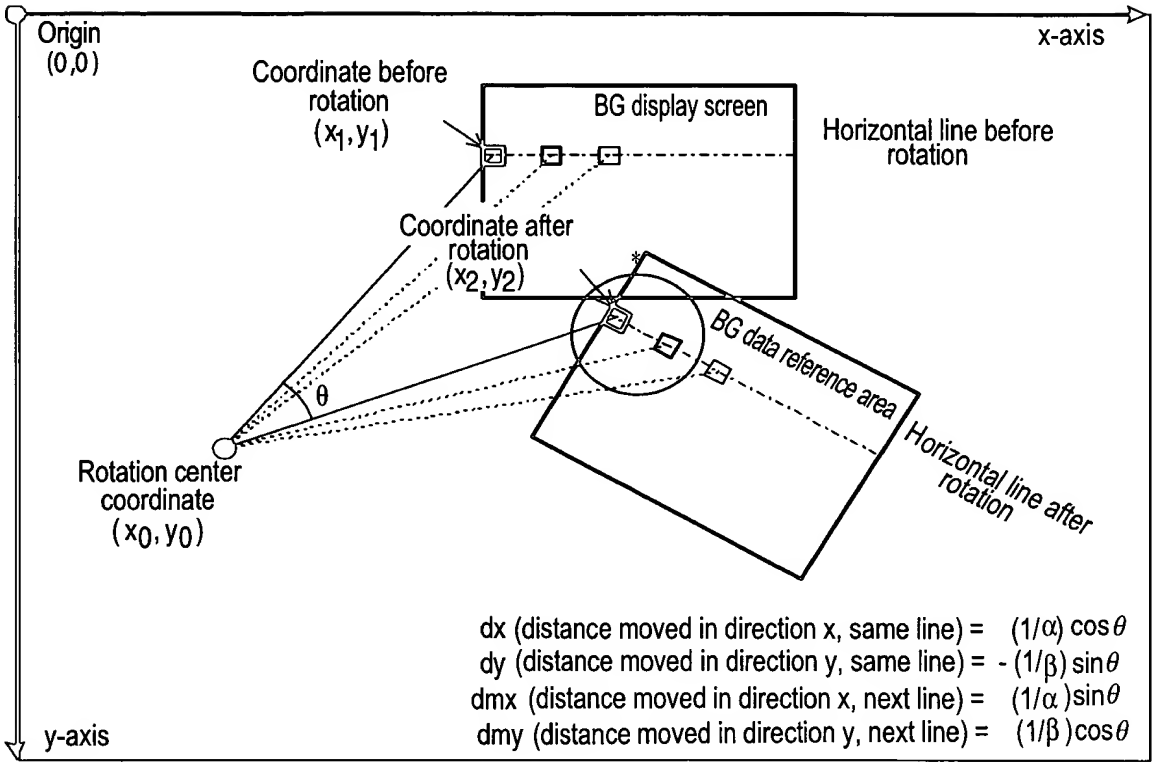

1024 dots
(128 blocks)
240 dots
(30 blocks)
160 dots
(20 blocks)
1024 dots
(128 blocks)
000h 001h 002h 003h 004h 01Dh 01Eh 07Eh 07Fh
080h 081h 082h 083h 084h 09Dh 09Eh 0FEh 0FFh
100h 101h 102h 103h 104h 11Dh 11Eh 17Eh 17Fh
180h 181h 182h 183h 184h 19Dh 19Eh 1FEh 1FFh
980h 981h 982h 983h 984h 99Dh 99Eh 9FEh 9FFh
A00h A01h A02h A03h A04h A1Dh A1Eh A7Eh A7Fh
3F00h 3F01h 3F02h 3F03h 3F04h 3F1Dh 3F1Eh 3F7Eh 3F7Fh
3F80h 3F81h 3F82h 3F83h 3F84h 3F9Dh 3F9Eh 3FFEh 3FFFh
LCD Display Area

Fig. 41D



α: Magnification along x-axi
β: Magnification along y-axi

Fig. 42A

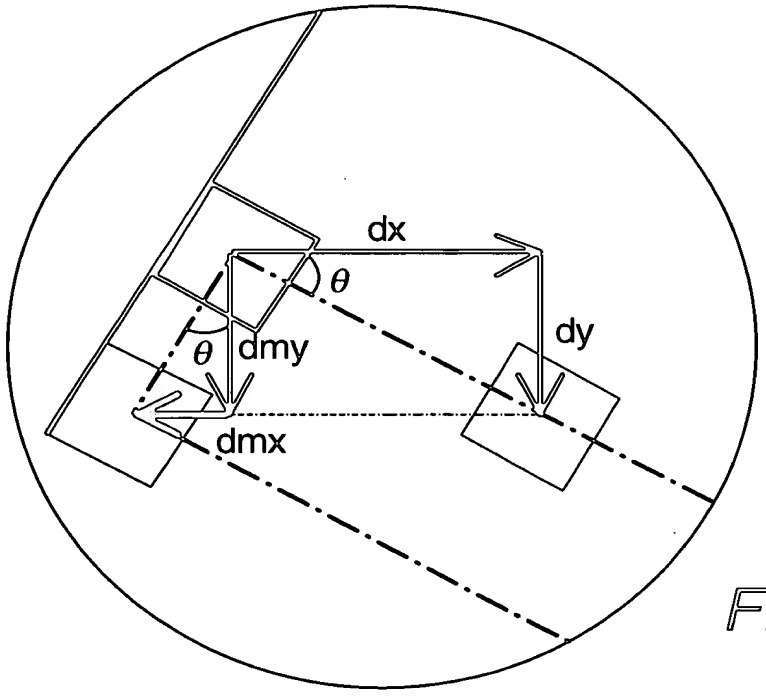


Fig. 42B

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
028h 038h	BG2X_L BG3X_L	X-coordinate of reference starting point (rotation/scaling results)	W	0000h

Fig.43A

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
02Ah 03Ah	BG2X_H BG3X_H	X-coordinate of reference starting point (rotation/scaling results)	W	0000h

Fig.43B

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
02Ch 03Ch	BG2Y_L BG3Y_L	Y-coordinate of reference starting point (rotation/scaling results)	W	0000h

Fig.43C

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
02Eh 03Eh	BG2Y_H BG3Y_H	Y-coordinate of reference starting point (rotation/scaling results)	W	0000h

Fig.43D

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
020h 030h	BG2PA BG3PA	dx: distance of movement in x direction along same line	W	0100h

Fig.44A

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
022h 032h	BG2PB BG3PB	dmx: distance of movement in x direction along next line	W	0000h

Fig.44B

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
024h 034h	BG2PC BG3PC	dy: distance of movement in y direction along same line	W	0000h

Fig.44C

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
026h 036h	BG2PD BG3PD	dmy: distance of movement in y direction along next line	W	0100h

Fig.44D

Offset Settings Registers

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
010h	BG0HOFS	H offset	W	0000h
014h	BG1HOFS			
018h	BG2HOFS			
01Ch	BG3HOFS			

Fig.45A

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
012h	BG0VOFS	V offset	W	0000h
016h	BG1VOFS			
01Ah	BG2VOFS			
01Eh	BG3VOFS			

Fig.45B

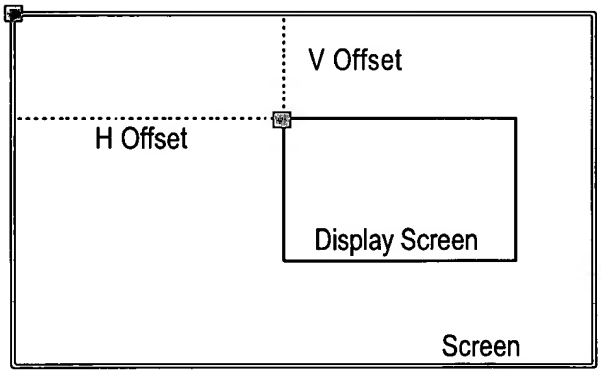


Fig.46

Address	Register	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00	Attributes	Initial Value
00Ch	BG2CNT	0 0 Priority Specification / Mosaic	R/W	0000h

Mosaic
0: Disable
1: Enable

Priority Specification
00: 1st priority
01: 2nd priority
10: 3rd priority
11: 4th priority

Fig.47

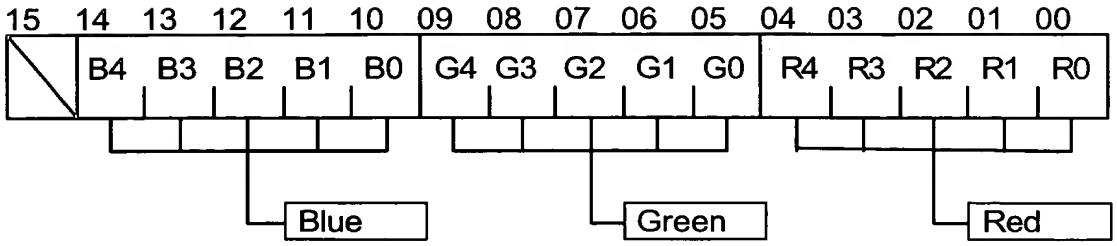


Fig.48A

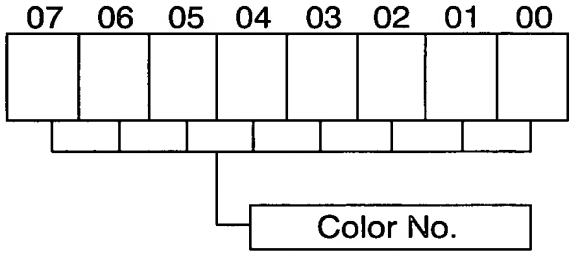


Fig. 48B

	0	1	2	3	4	▫▫▫	236	237	238	239
0	0h	2h	4h	6h	8h	▫▫▫	1D8h	1Dah	1DCh	1DEh
1	1E0h	1E2h	1E4h	1E6h	1E8h	▫▫▫	3B8h	3Bah	3BCh	3BEh
2	3C0h	3C2h	3C4h	3C6h	3C8h	▫▫▫	598h	59Ah	59Ch	59Eh
3	5A0h	5A2h	5A4h	5A6h	5A8h	▫▫▫	778h	77Ah	77Ch	7Eh
4	780h	782h	784h	786h	788h	▫▫▫	958h	95Ah	95Ch	95Eh
|	|	|	|	|	|	|	|	|	|	|
156	12480h	12482h	12484h	12486h	12488h	▫▫▫	12658h	1265Ah	1265Ch	1265Eh
157	12660h	12662h	12664h	12666h	12668h	▫▫▫	12838h	1283Ah	1283Ch	1283Eh
158	12840h	12842h	12844h	12846h	12848h	▫▫▫	12A18h	12A1Ah	12A1Ch	12A1Eh
159	12A20h	12A22h	12A24h	12A26h	12A28h	▫▫▫	12BF8h	12BFAh	12BFCh	12BFEh

VRAM address (+06000000h)

Fig.49

Frame 0

	0	1	2	3	4	▪▪▪	236	237	238	239
0	0h	1h	2h	3h	4h	•••	ECh	EDh	EEh	EFh
1	F0h	F1h	F2h	F3h	F4h	•••	1DCh	1DDh	1DEh	1DFh
2	1E0h	1E1h	1E2h	1E3h	1E4h	•••	2CCh	2CDh	2CEh	2CFh
3	2D0h	2D1h	2D2h	2D3h	2D4h	•••	3BCh	3BDh	3BEh	3BFh
4	3C0h	3C1h	3C2h	3C3h	3C4h	•••	4ACh	4ADh	4AEh	4AFh
|	|	|	|	|	|	|	|	|	|	|
156	9240h	9241h	9242h	9243h	9244h	•••	932Ch	932Dh	932Eh	932Fh
157	9330h	9331h	9332h	9333h	9334h	•••	941Ch	941Dh	941Eh	941Fh
158	9420h	9421h	9422h	9423h	9424h	•••	950Ch	950Dh	950Eh	950Fh
159	9510h	9511h	9512h	9513h	9514h	•••	95FCh	95FDh	95FEh	95FFh

VRAM address (+06000000h)

Fig. 50A

Frame 1

	0	1	2	3	4	▪▪▪	236	237	238	239
0	A000h	A001h	A002h	A003h	A004h	•••	A0ECh	A0EDh	A0EEh	A0EFh
1	A0F0h	A0F1h	A0F2h	A0F3h	A0F4h	•••	A1DCh	A1DDh	A1DEh	A1DFh
2	A1E0h	A1E1h	A1E2h	A1E3h	A1E4h	•••	A2CCh	A2CDh	A2CEh	A2CFh
3	A2D0h	A 2D1h	A2D2h	A 2D3h	A2D4h	•••	A3BCh	A3BDh	A3BEh	A3BFh
4	A3C0h	A 3C1h	A3C2h	A 3C3h	A3C4h	•••	A4ACh	A4ADh	A4AEh	A 4AFh
|	|	|	|	|	|	|	|	|	|	|
156	13240h	13241h	13242h	13243h	13244h	•••	1332Ch	1332Dh	1332Eh	1332Fh
157	13330h	13331h	13332h	13333h	13334h	•••	1341Ch	1341Dh	1341Eh	1341Fh
158	13420h	13421h	13422h	13423h	13424h	•••	1350Ch	1350Dh	1350Eh	1350Fh
159	13510h	13511h	13512h	13513h	13514h	•••	135FCh	135FDh	135FEh	135FFh

VRAM address (+06000000h)

Fig. 50B

Fig. 51A

Frame 0

	0	1	2	3	4	···	156	157	158	159
0	0h	2h	4h	6h	8h	···	138h	13Ah	13Ch	13Eh
1	140h	142h	144h	146h	148h	···	298h	29Ah	29Ch	29Eh
2	2A0h	2A2h	2A4h	2A6h	2A8h	···	3B8h	3BAh	3BCh	3BEh
3	3C0h	3C2h	3C4h	3C6h	3C8h	···	4F8h	4FAh	4FCh	4FEh
4	500h	502h	504h	506h	508h	···	638h	63Ah	63Ch	63Eh
|	|	|	|	|	|	|	|	|	|	|
124	9B00h	9B02h	9B04h	9B06h	9B08h	···	9C38h	9C3Ah	9C3Ch	9C3Eh
125	9C40h	9C42h	9C44h	9C46h	9C48h	···	9D78h	9D7Ah	9D7Ch	9D7Eh
126	9D80h	9D82h	9D84h	9D86h	9D88h	···	9EB8h	9EBAh	9EBCh	9EBEh
127	9EC0h	9EC2h	9EC4h	9EC6h	9EC8h	···	9FF8h	9FFAh	9FFCh	9FFEh

VRAM Address (+06000000h)

Fig. 51B

Frame 1

	0	1	2	3	4	···	156	157	158	159
0	A000h	A002h	A004h	A006h	A008h	···	A138h	A13Ah	A13Ch	A13Eh
1	A140h	A142h	A144h	A146h	A148h	···	A298h	A29Ah	A29Ch	A29Eh
2	A2A0h	A2A2h	A2A4h	A2A6h	A2A8h	···	A3B8h	A3BAh	A3BCh	A3BEh
3	A3C0h	A3C2h	A3C4h	A3C6h	A3C8h	···	A4F8h	A4FAh	A4FCh	A4FEh
4	A500h	A502h	A504h	A506h	A508h	···	A638h	A63Ah	A63Ch	A63Eh
|	|	|	|	|	|	|	|	|	|	|
124	13B00h	13B02h	13B04h	13B06h	13B08h	···	13C38h	13C3Ah	13C3Ch	13C3Eh
125	13C40h	13C42h	13C44h	13C46h	13C48h	···	13D78h	13D7Ah	13D7Ch	13D7Eh
126	13D80h	13D82h	13D84h	13D86h	13D88h	···	13EB8h	13EBAh	13EBCh	13EBEh
127	13EC0h	13EC2h	13EC4h	13EC6h	13EC8h	···	13FF8h	13FFAh	13FFCh	13FFEh

VRAM address (+06000000h)

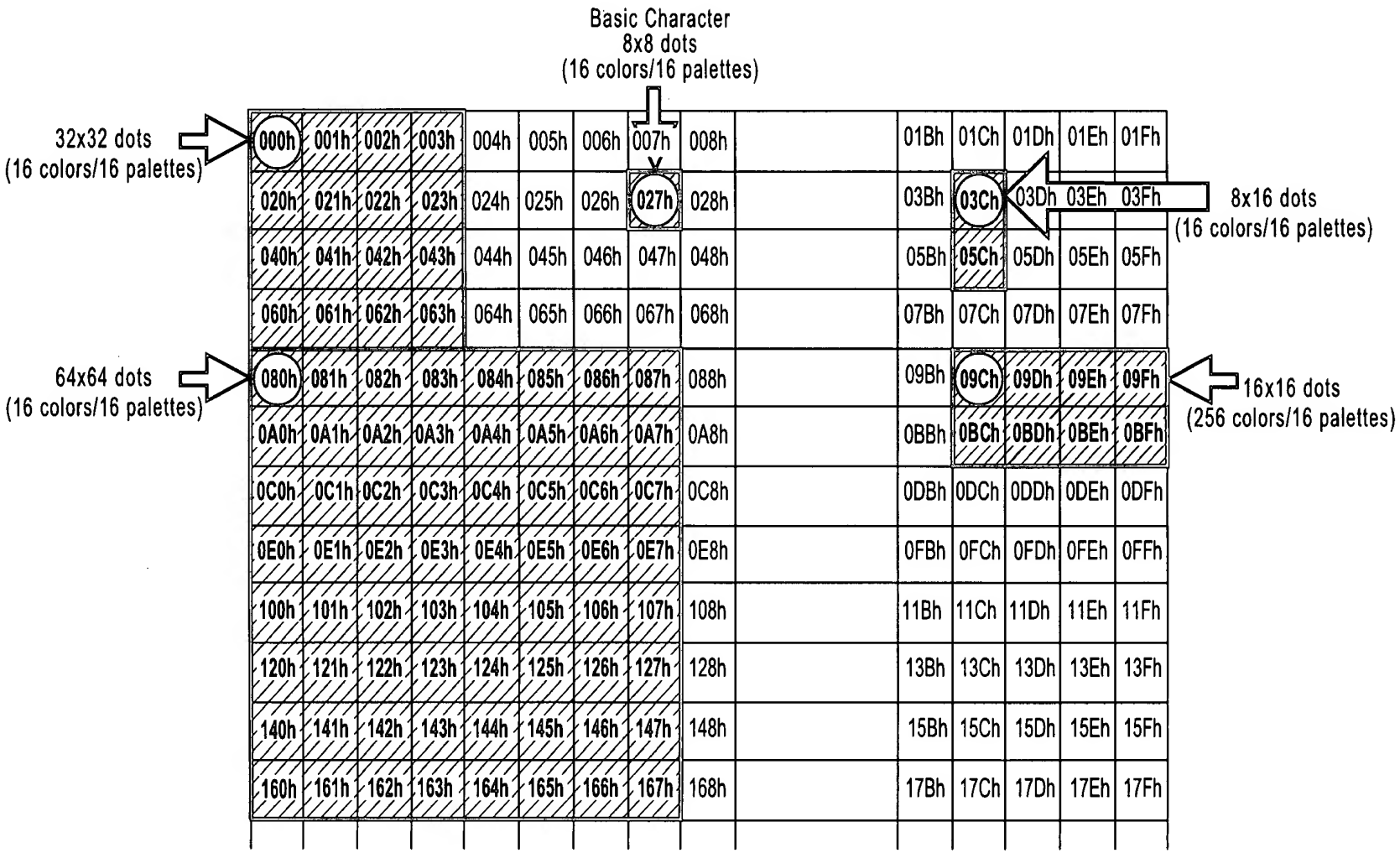

Basic Character
8x8 dots
(16 colors/16 palettes)
32x32 dots
(16 colors/16 palettes)
64x64 dots
(16 colors/16 palettes)
8x16 dots
(16 colors/16 palettes)
16x16 dots
(256 colors/16 palettes)
000h 001h 002h 003h 004h 005h 006h 007h 008h 01Bh 01Ch 01Dh 01Eh 01Fh
020h 021h 022h 023h 024h 025h 026h 027h 028h 03Bh 03Ch 03Dh 03Eh 03Fh
040h 041h 042h 043h 044h 045h 046h 047h 048h 05Bh 05Ch 05Dh 05Eh 05Fh
060h 061h 062h 063h 064h 065h 066h 067h 068h 07Bh 07Ch 07Dh 07Eh 07Fh
080h 081h 082h 083h 084h 085h 086h 087h 088h 09Bh 09Ch 09Dh 09Eh 09Fh
0A0h 0A1h 0A2h 0A3h 0A4h 0A5h 0A6h 0A7h 0A8h 0BBh 0BCh 0BDh 0BEh 0BFh
0C0h 0C1h 0C2h 0C3h 0C4h 0C5h 0C6h 0C7h 0C8h 0DBh 0DCh 0DDh 0DEh 0DFh
0E0h 0E1h 0E2h 0E3h 0E4h 0E5h 0E6h 0E7h 0E8h 0FBh 0FCh 0FDh 0FEh 0FFh
100h 101h 102h 103h 104h 105h 106h 107h 108h 11Bh 11Ch 11Dh 11Eh 11Fh
120h 121h 122h 123h 124h 125h 126h 127h 128h 13Bh 13Ch 13Dh 13Eh 13Fh
140h 141h 142h 143h 144h 145h 146h 147h 148h 15Bh 15Ch 15Dh 15Eh 15Fh
160h 161h 162h 163h 164h 165h 166h 167h 168h 17Bh 17Ch 17Dh 17Eh 17Fh
Character mapping area (character no. in hexadecimal notation)
Character name

Fig. 52

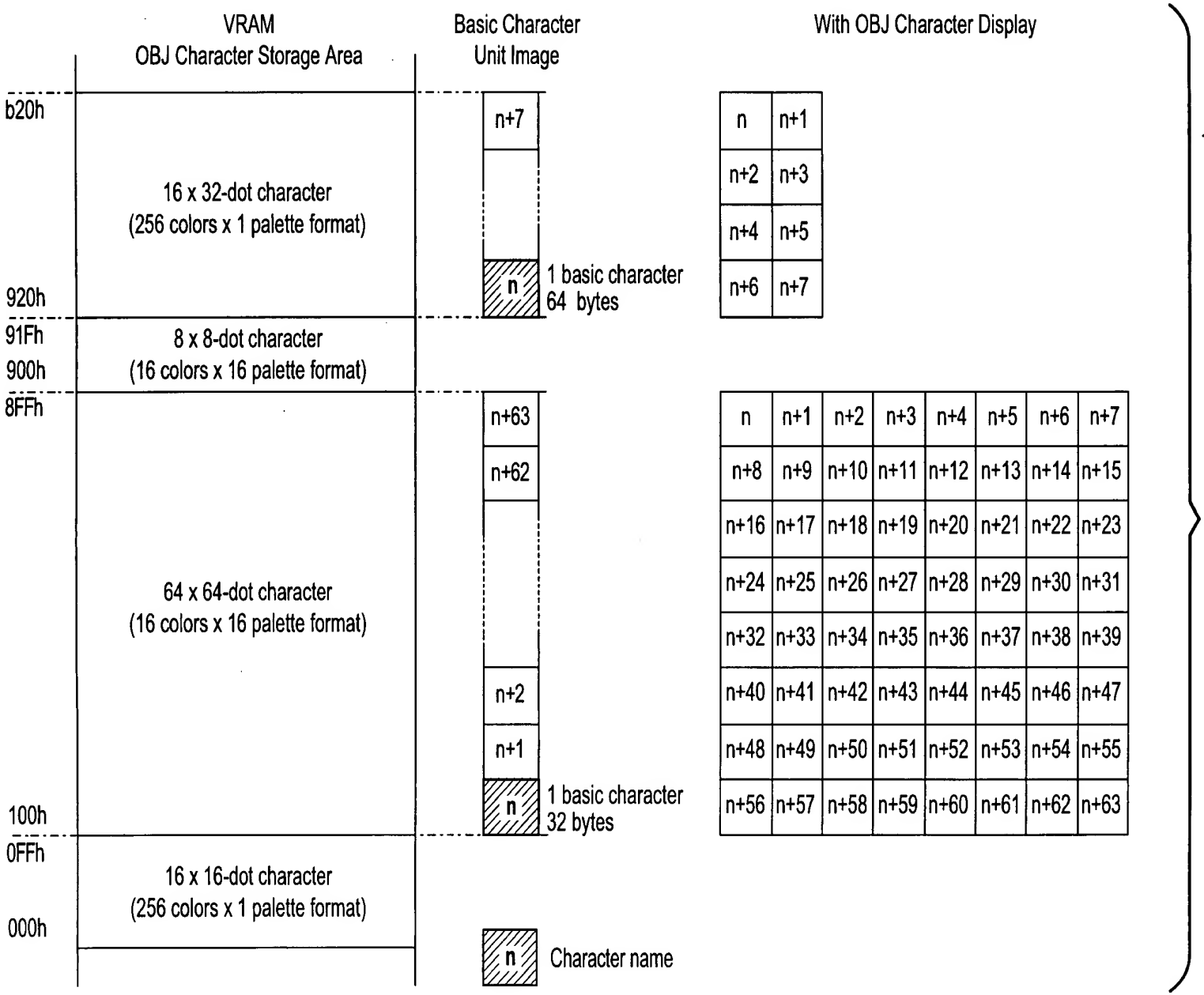

VRAM
OBJ Character Storage Area
Basic Character
Unit Image
With OBJ Character Display
b20h
16 x 32-dot character
(256 colors x 1 palette format)
920h
91Fh
8 x 8-dot character
(16 colors x 16 palette format)
900h
8FFh
64 x 64-dot character
(16 colors x 16 palette format)
100h
0FFh
16 x 16-dot character
(256 colors x 1 palette format)
000h
n+7
n
1 basic character
64 bytes
n+63
n+62
n+2
n+1
n
1 basic character
32 bytes
n
Character name
n n+1
n+2 n+3
n+4 n+5
n+6 n+7
n n+1 n+2 n+3 n+4 n+5 n+6 n+7
n+8 n+9 n+10 n+11 n+12 n+13 n+14 n+15
n+16 n+17 n+18 n+19 n+20 n+21 n+22 n+23
n+24 n+25 n+26 n+27 n+28 n+29 n+30 n+31
n+32 n+33 n+34 n+35 n+36 n+37 n+38 n+39
n+40 n+41 n+42 n+43 n+44 n+45 n+46 n+47
n+48 n+49 n+50 n+51 n+52 n+53 n+54 n+55
n+56 n+57 n+58 n+59 n+60 n+61 n+62 n+63

Fig. 53

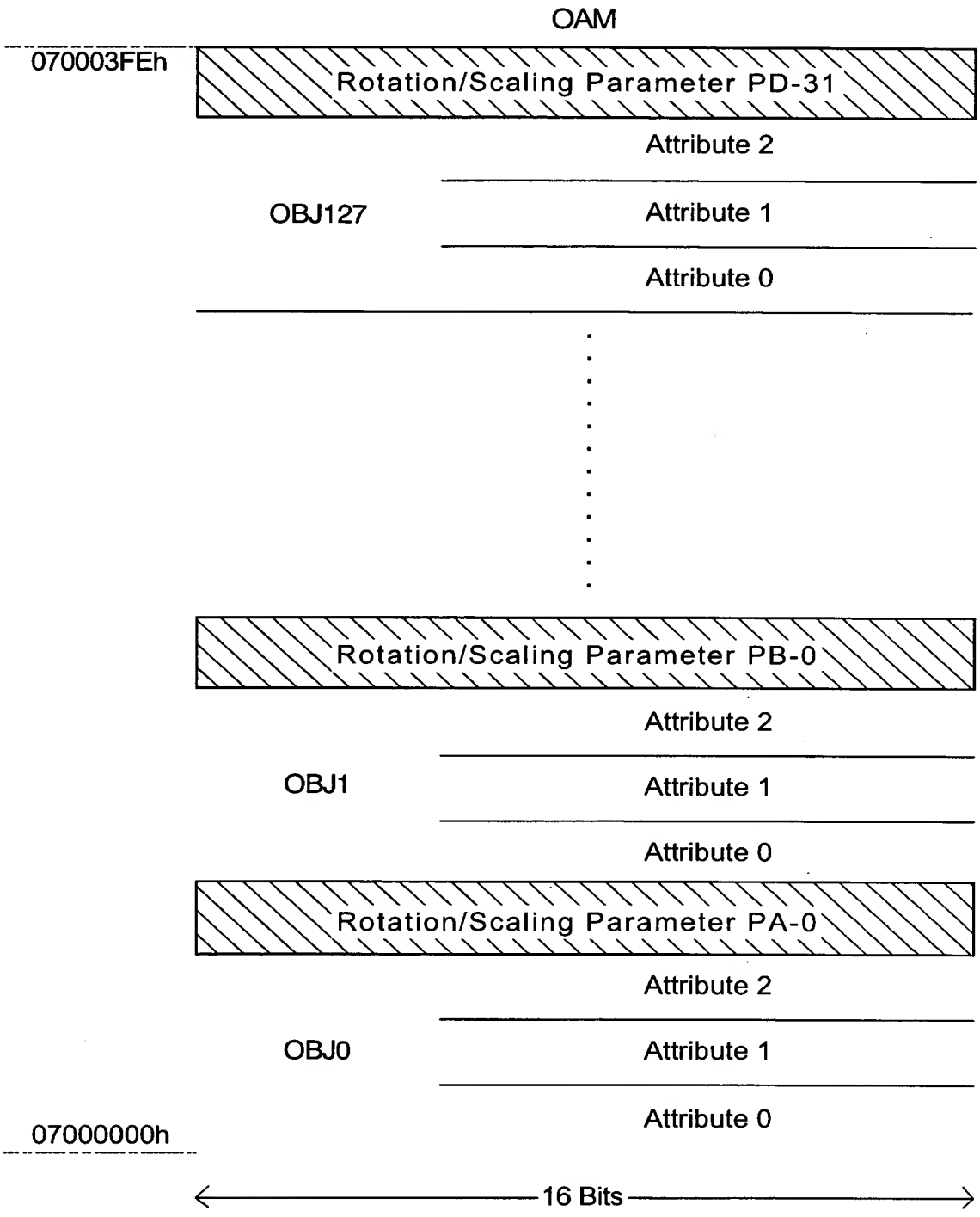

OAM
070003FEh
Rotation/Scaling Parameter PD-31
Attribute 2
OBJ127
Attribute 1
Attribute 0
Rotation/Scaling Parameter PB-0
Attribute 2
OBJ1
Attribute 1
Attribute 0
Rotation/Scaling Parameter PA-0
Attribute 2
OBJ0
Attribute 1
Attribute 0
07000000h
16 Bits

Fig. 54

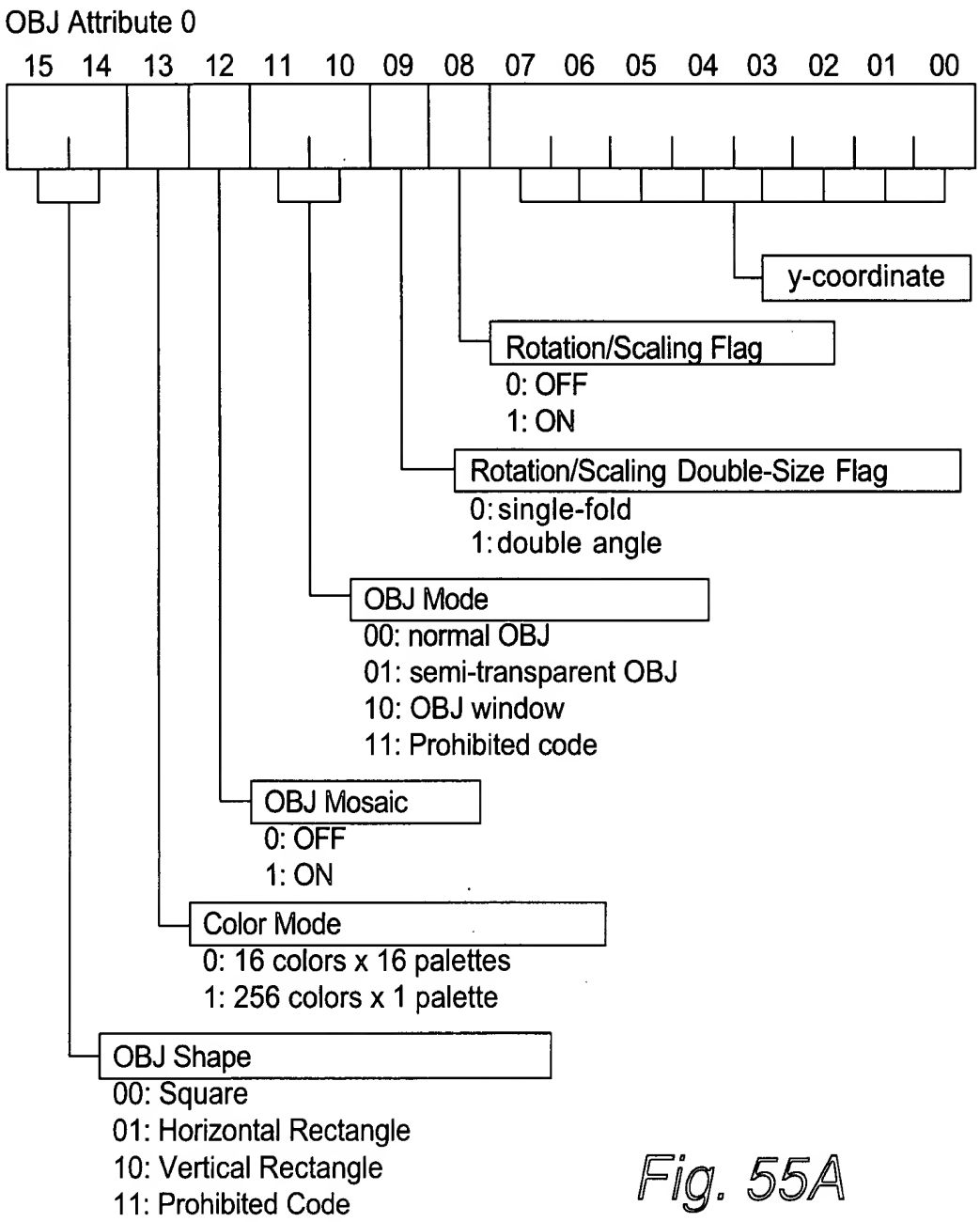


Fig. 55A

OBJ Attribute 1

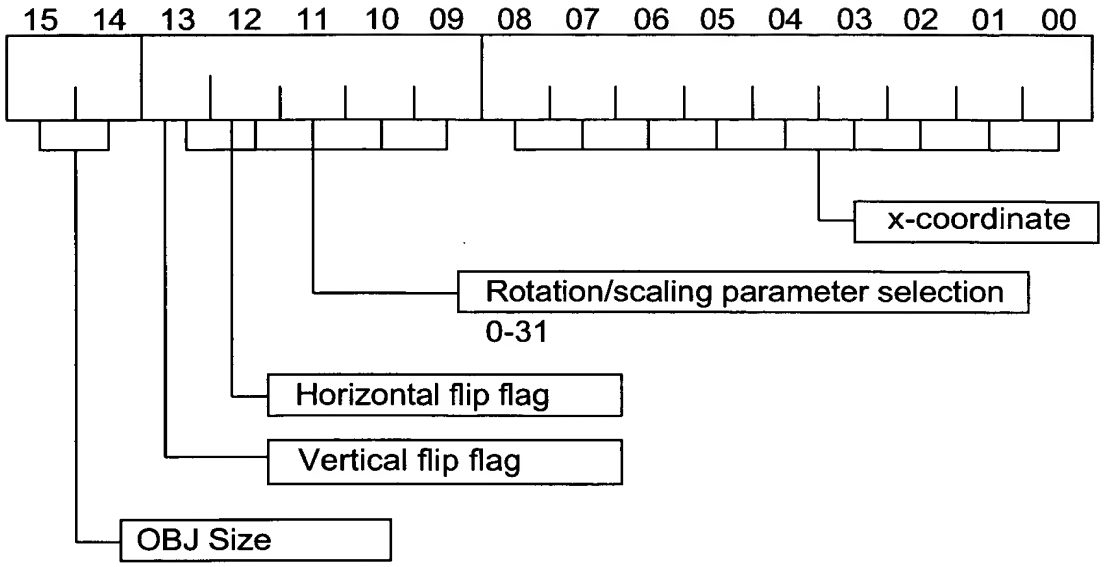


Fig. 55B

OBJ Attribute 2

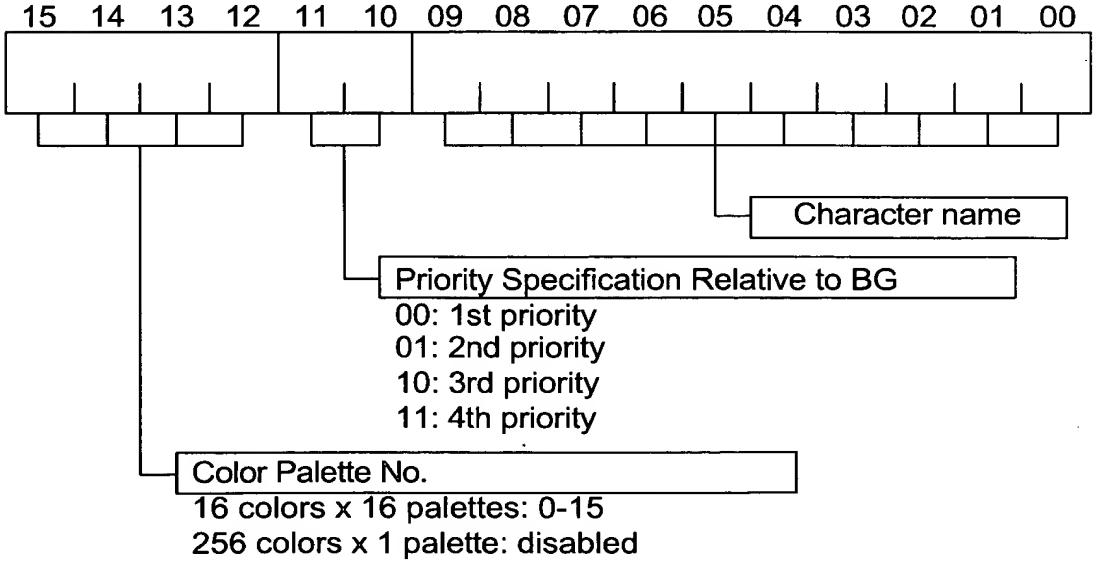


Fig. 55C

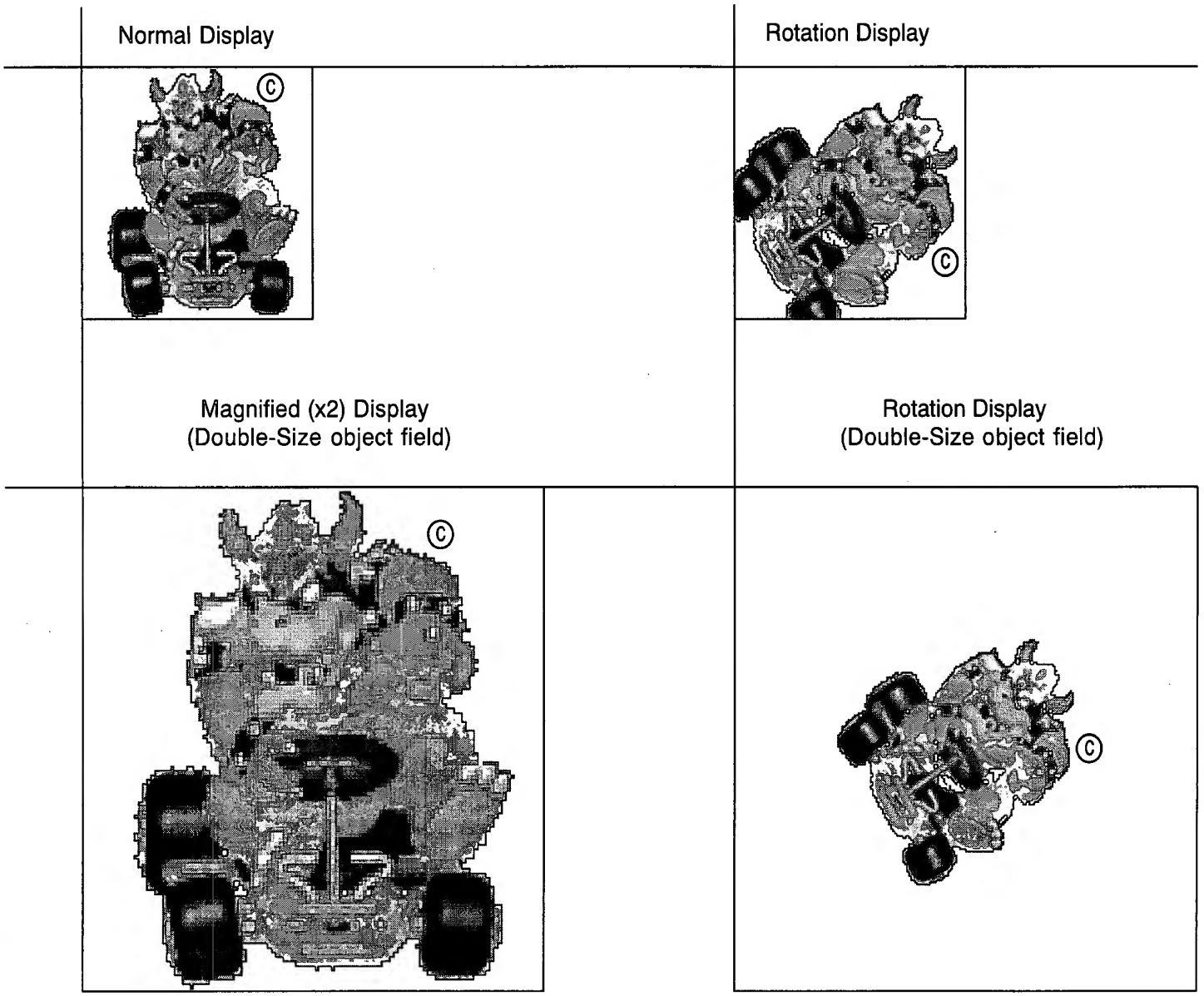


Fig. 56

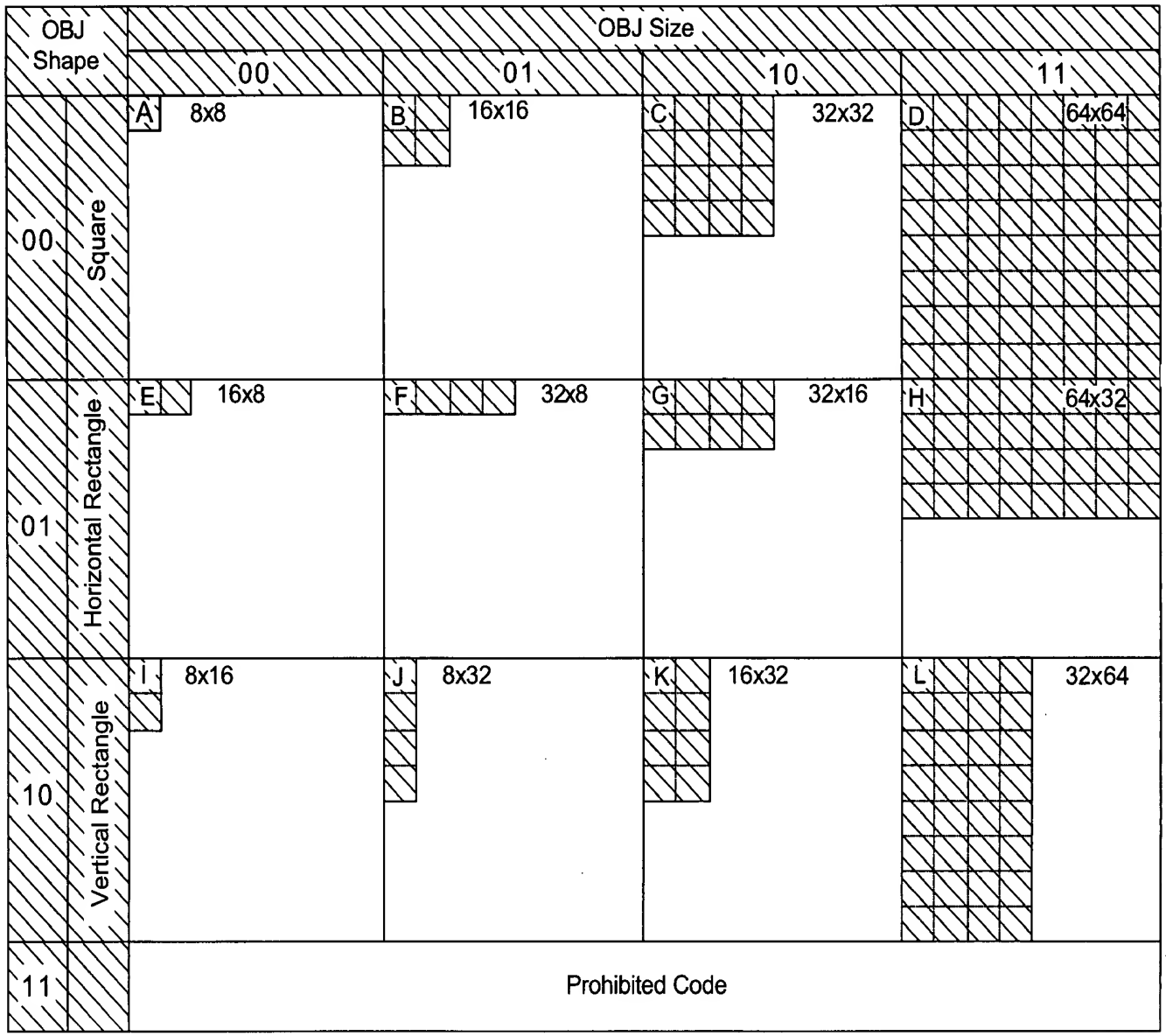

OBJ Shape
OBJ Size
00
01
10
11
00
Square
01
Horizontal Rectangle
10
Vertical Rectangle
11
A
8x8
B
16x16
C
32x32
D
64x64
E
16x8
F
32x8
G
32x16
H
64x32
I
8x16
J
8x32
K
16x32
L
32x64
Prohibited Code

Fig. 57

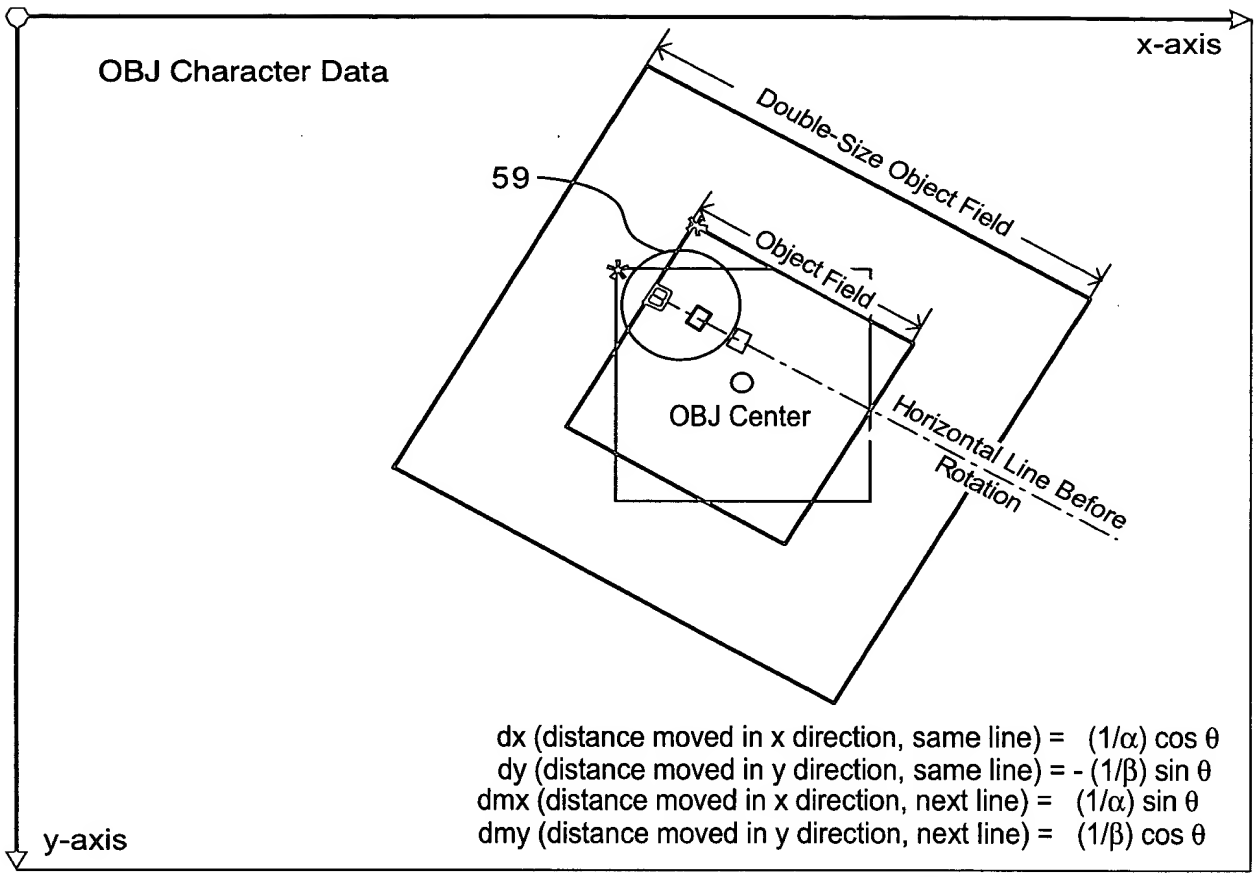


Fig. 58A

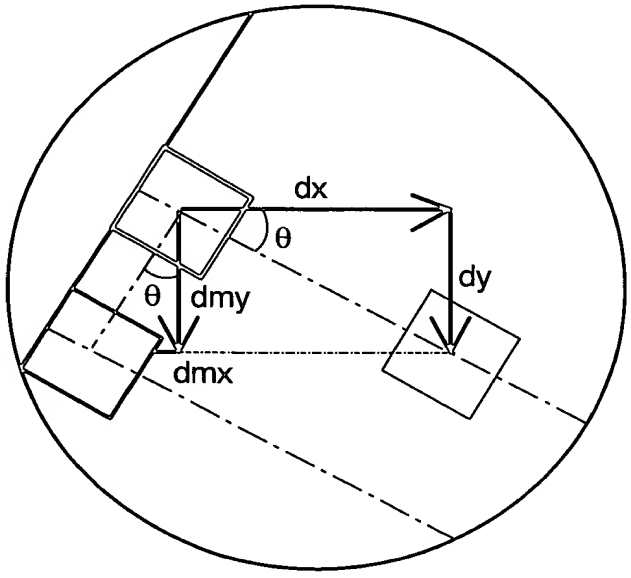


Fig. 58B

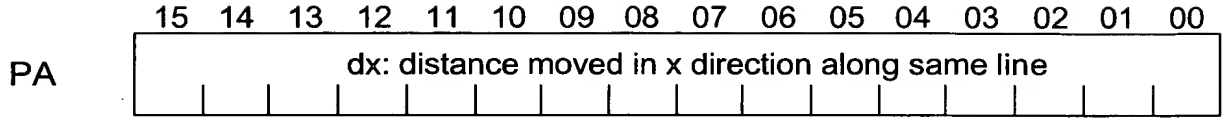


Fig. 59A

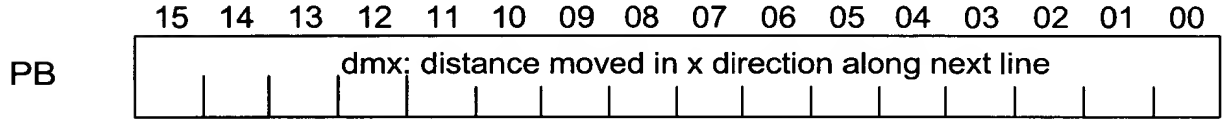


Fig. 59B

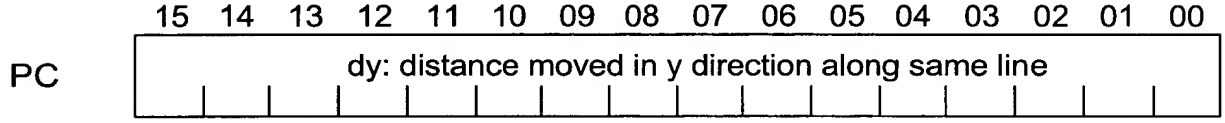


Fig. 59C

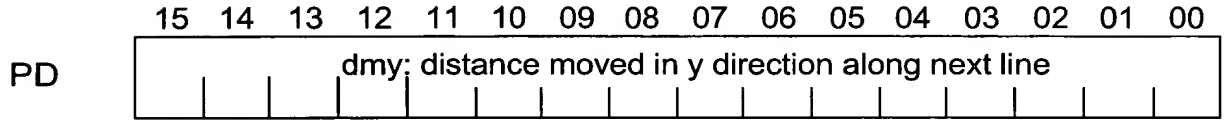


Fig. 59D

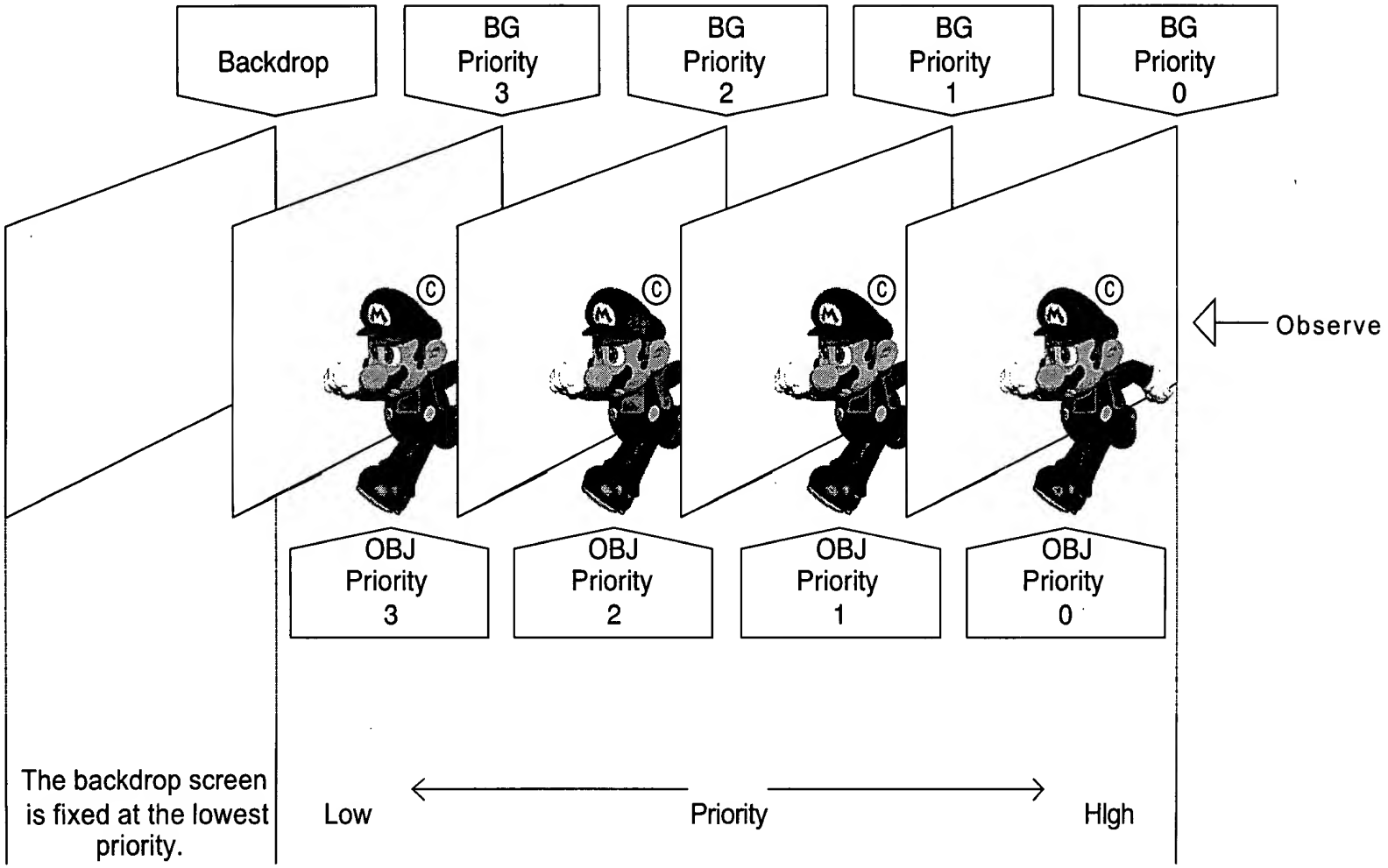


Fig. 60

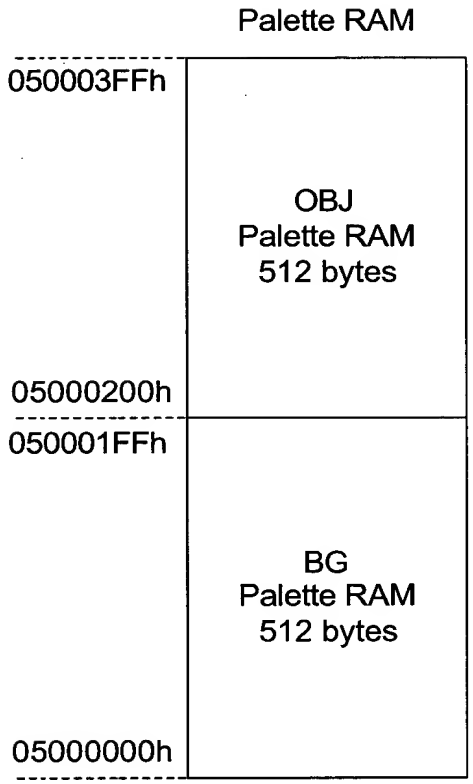

Palette RAM
050003FFh
OBJ
Palette RAM
512 bytes
05000200h
050001FFh
BG
Palette RAM
512 bytes
05000000h

Fig. 61

16 Colors x 16 Palettes

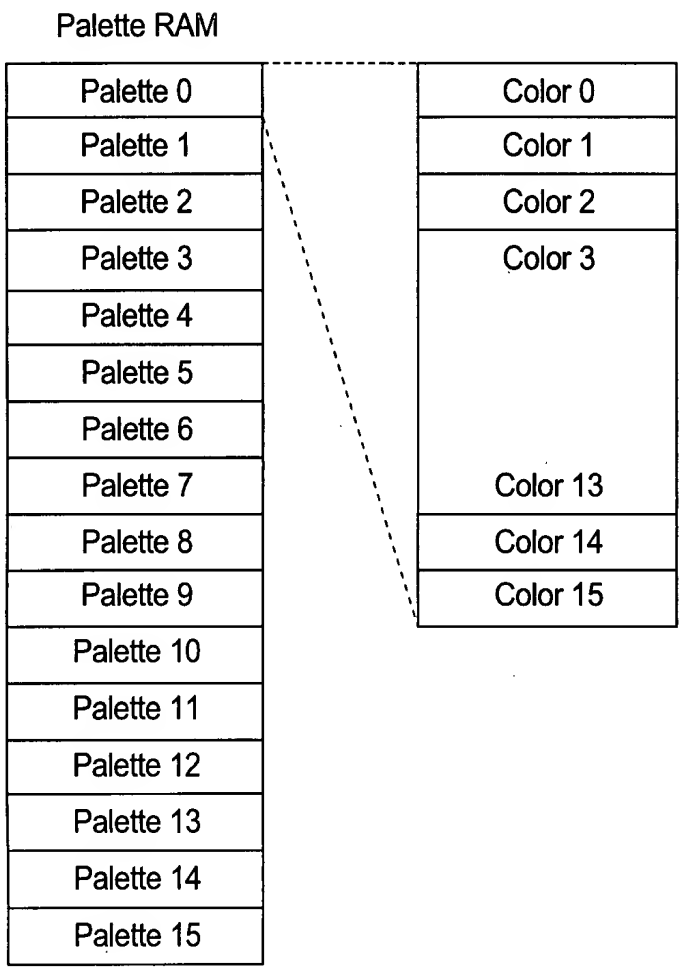


Fig. 62A

256 Colors x 1 Palette

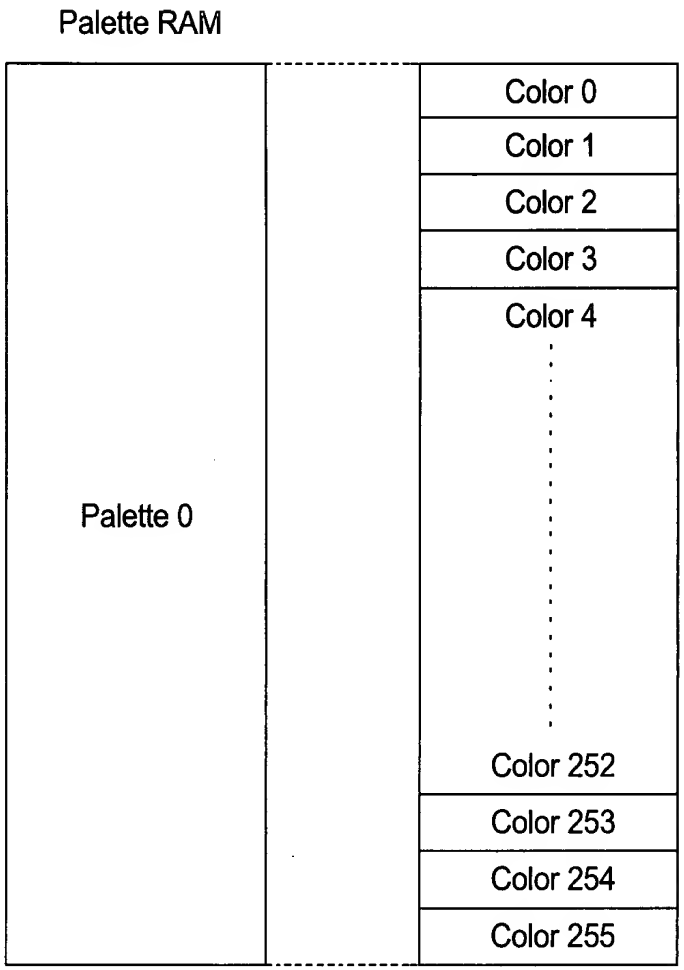


Fig. 62B

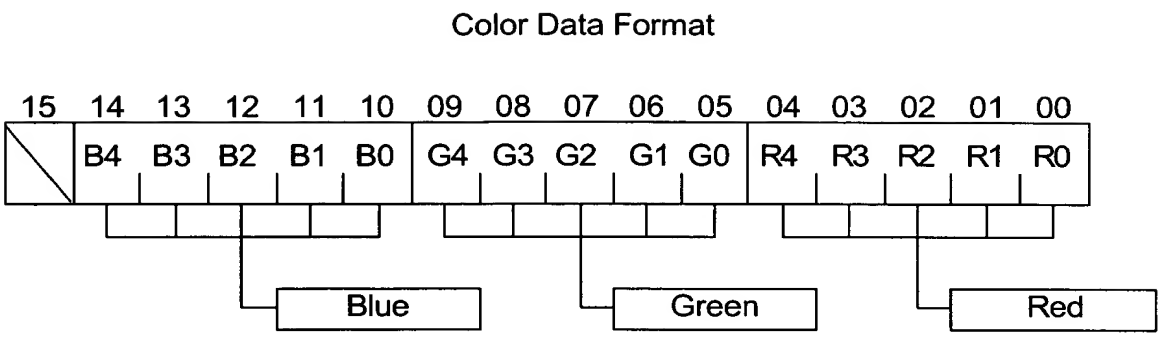

Color Data Format
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
B4 B3 B2 B1 B0 G4 G3 G2 G1 G0 R4 R3 R2 R1 R0
Blue
Green
Red

Fig. 63

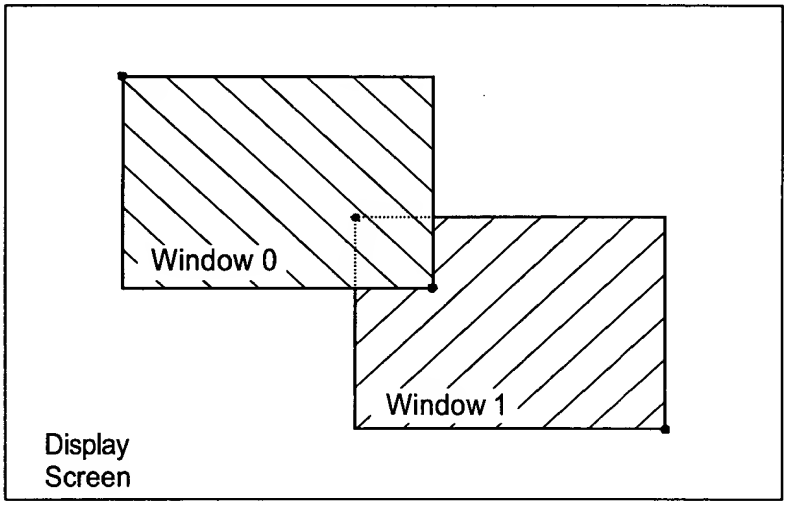

Window 0
Window 1
Display
Screen

Fig. 64

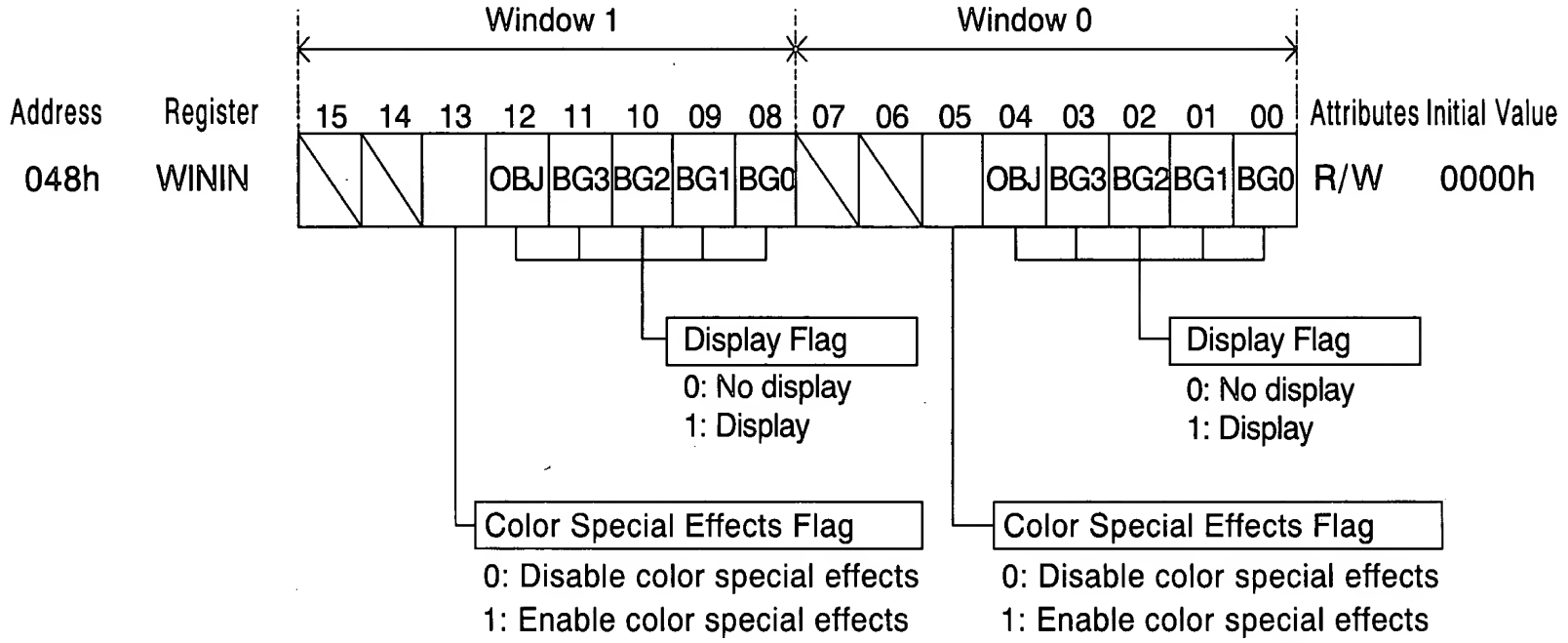

Window 1
Window 0
Address
Register
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Attributes
Initial Value
048h
WININ
OBJ BG3 BG2 BG1 BG0
OBJ BG3 BG2 BG1 BG0
R/W
0000h
Display Flag
0: No display
1: Display
Display Flag
0: No display
1: Display
Color Special Effects Flag
0: Disable color special effects
1: Enable color special effects
Color Special Effects Flag
0: Disable color special effects
1: Enable color special effects

Fig. 65

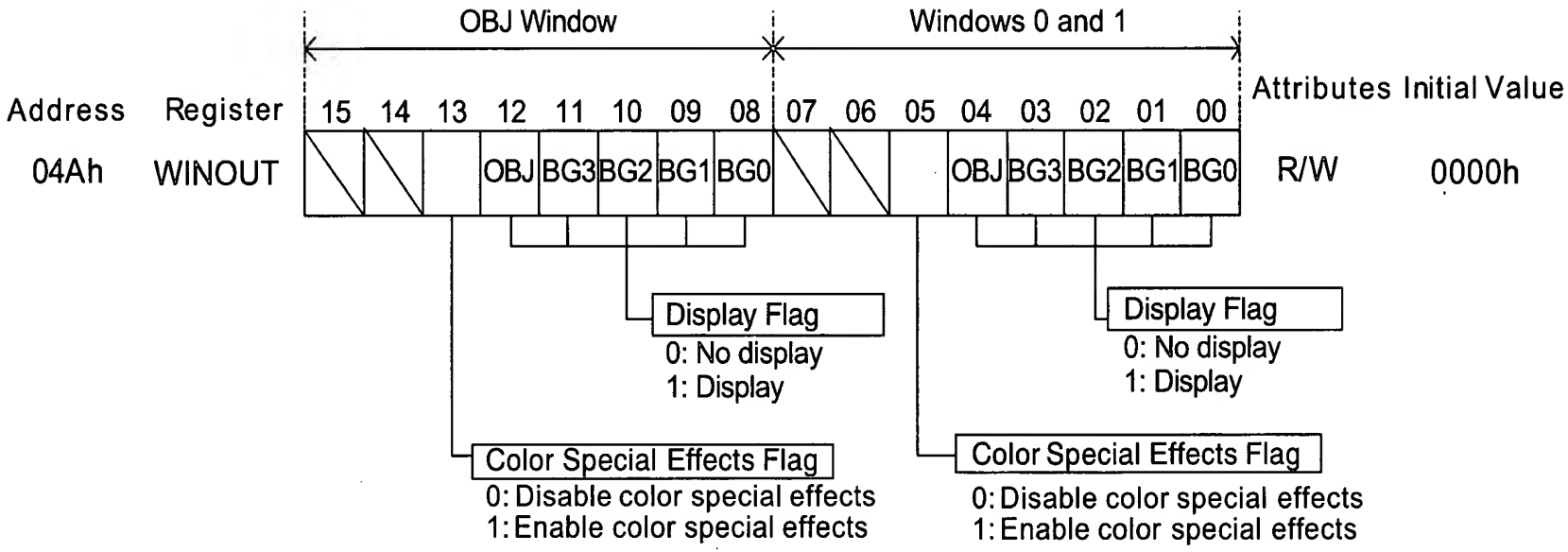

OBJ Window
Windows 0 and 1
Address
Register
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Attributes
Initial Value
04Ah
WINOUT
OBJ BG3 BG2 BG1 BG0
OBJ BG3 BG2 BG1 BG0
R/W
0000h
Display Flag
0: No display
1: Display
Display Flag
0: No display
1: Display
Color Special Effects Flag
0: Disable color special effects
1: Enable color special effects
Color Special Effects Flag
0: Disable color special effects
1: Enable color special effects

Fig. 66

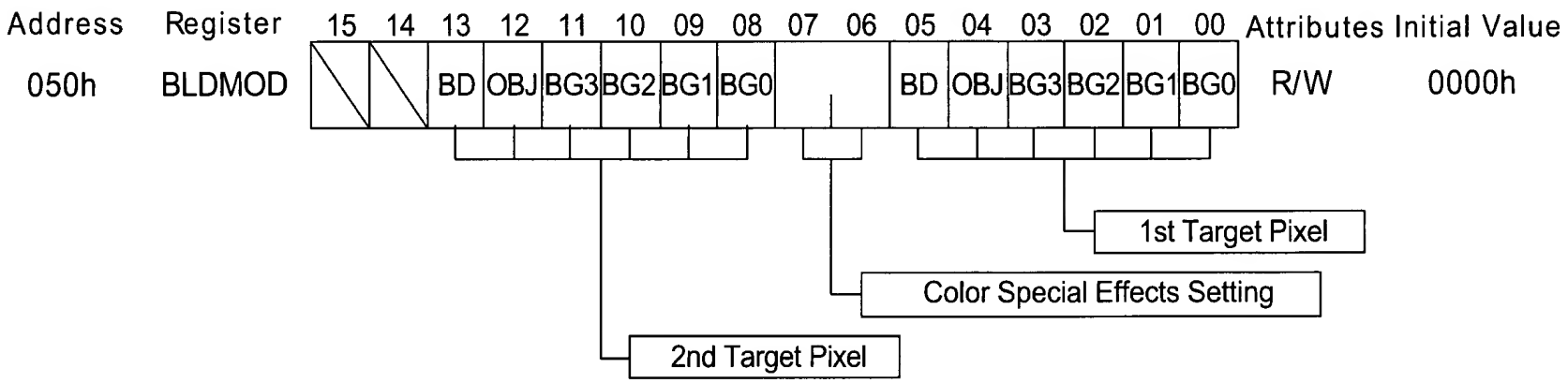

Address
Register
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Attributes
Initial Value
050h
BLDMOD
BD OBJ BG3 BG2 BG1 BG0
BD OBJ BG3 BG2 BG1 BG0
R/W
0000h
1st Target Pixel
Color Special Effects Setting
2nd Target Pixel

Fig. 67

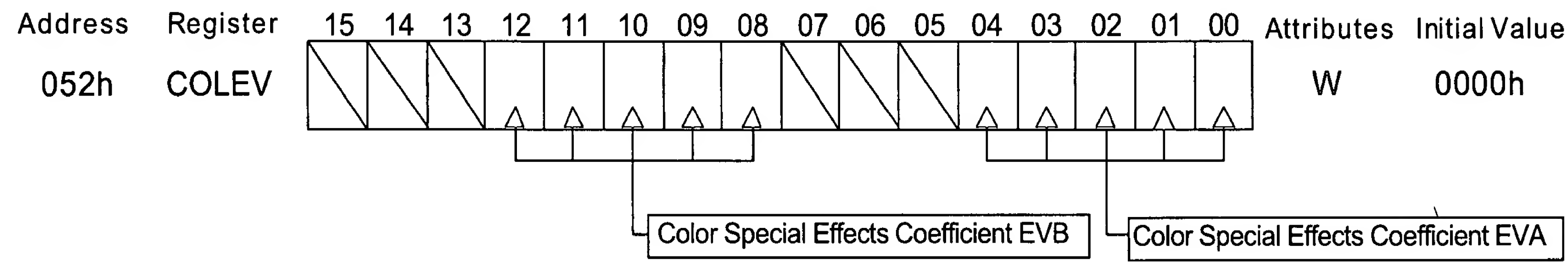


Fig. 68A

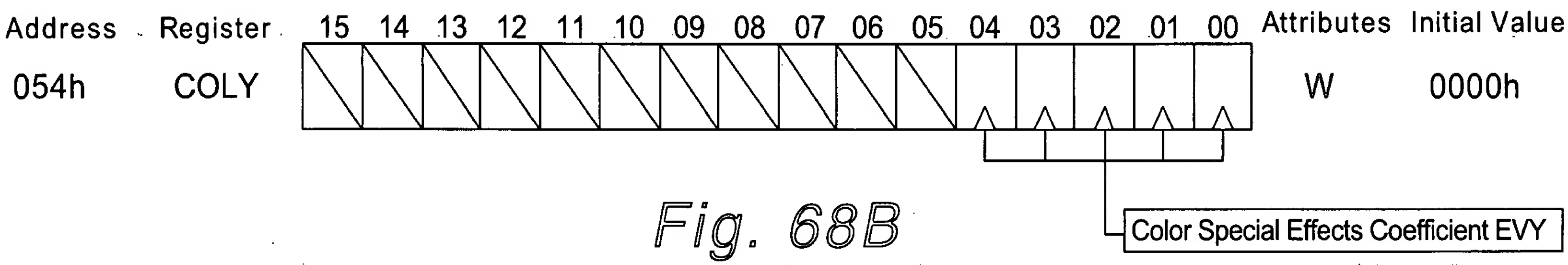


Fig. 68B

Fig. 69

EVA, EVB, EVY					Coeff.	EVA, EVB, EVY					Coeff.
0	0	0	0	0	0	0	1	0	0	0	8/16
0	0	0	0	1	1/16	0	1	0	0	1	9/16
0	0	0	1	0	2/16	0	1	0	1	0	10/16
0	0	0	1	1	3/16	0	1	0	1	1	11/16
0	0	1	0	0	4/16	0	1	1	0	0	12/16
0	0	1	0	1	5/16	0	1	1	0	1	13/16
0	0	1	1	0	6/16	0	1	1	1	0	14/16
0	0	1	1	1	7/16	0	1	1	1	1	15/16
						1	X	X	X	X	16/16

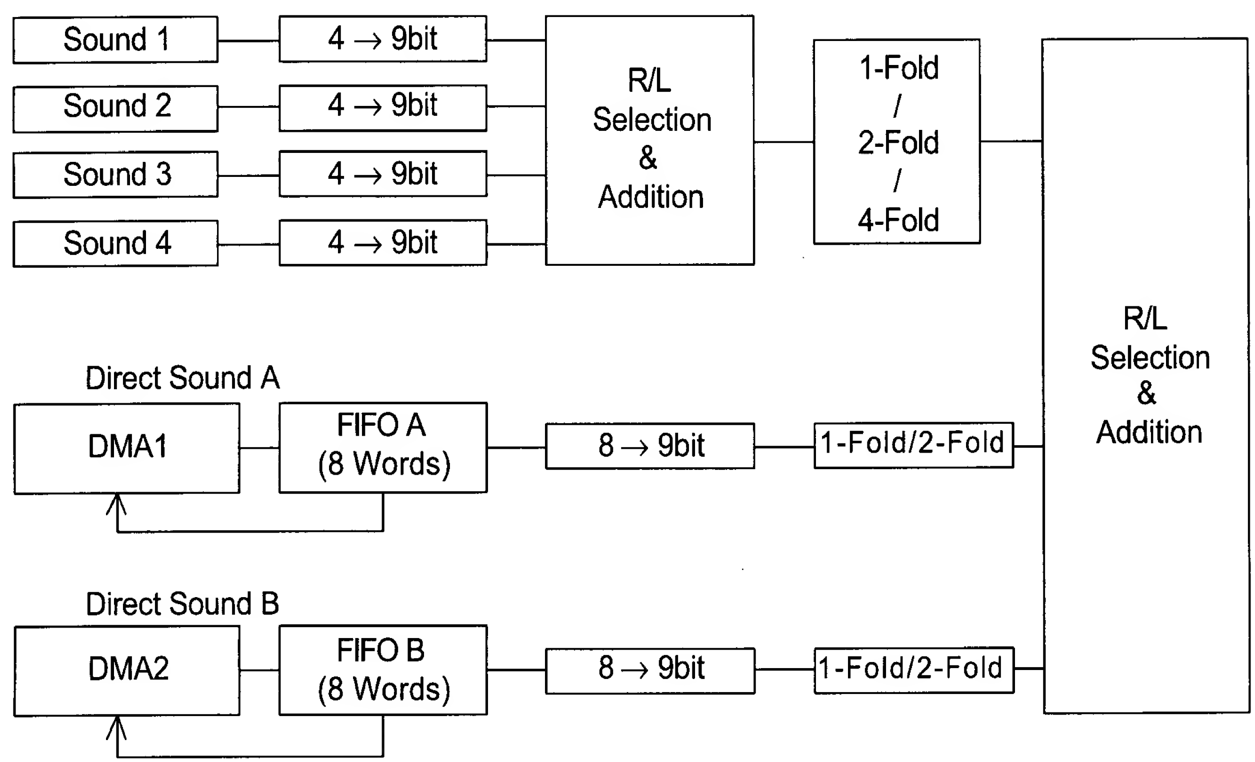

Sound 1
Sound 2
Sound 3
Sound 4
4 → 9bit
4 → 9bit
4 → 9bit
4 → 9bit
R/L Selection & Addition
1-Fold / 2-Fold / 4-Fold
Direct Sound A
DMA1
FIFO A (8 Words)
8 → 9bit
1-Fold/2-Fold
Direct Sound B
DMA2
FIFO B (8 Words)
8 → 9bit
1-Fold/2-Fold
R/L Selection & Addition

Fig. 70

Address	Register	15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00	Attributes	Initial Value
0A0h	SGFIFOA_L	Sound Data 1	Sound Data 0	W	-
0A4h	SGFIFOB_L				

Fig. 71A

Address	Register	15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00	Attributes	Initial Value
0A2h	SGFIFOA_H	Sound Data 3	Sound Data 2	W	-
0A6h	SGFIFOB_H				

Fig. 71B

Address	Register	15 14 13 12 11 10 09 08	07 06 05 04 03 02 01 00	Attributes	Intial Value
060h	SG10_L		NR10	R/W	0000h

No. of sweep shifts
0-7

Sweep Increase/Decrease
0: Addition (increase frequency)
1: Decrease (decrease frequency)

Sweep time

Fig. 72A

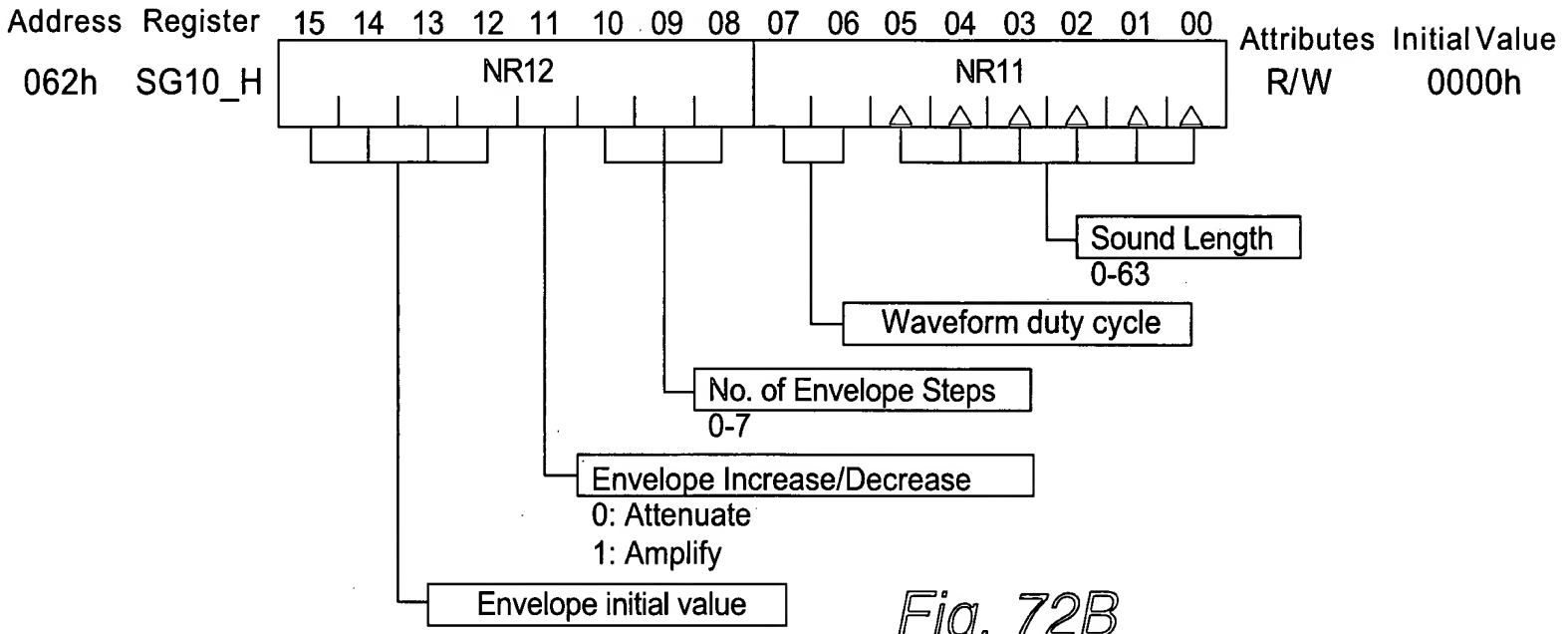


Fig. 72B

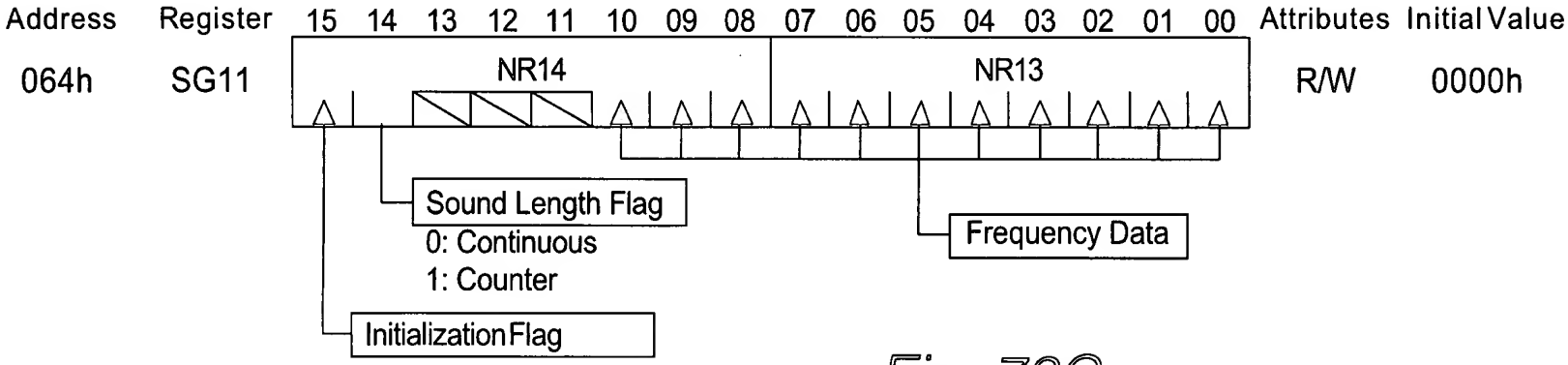


Fig. 72C

Setting	Duty Cycle	Waveform
00	12.5%	
01	25.0%	
10	50.0%	
11	75.0%	

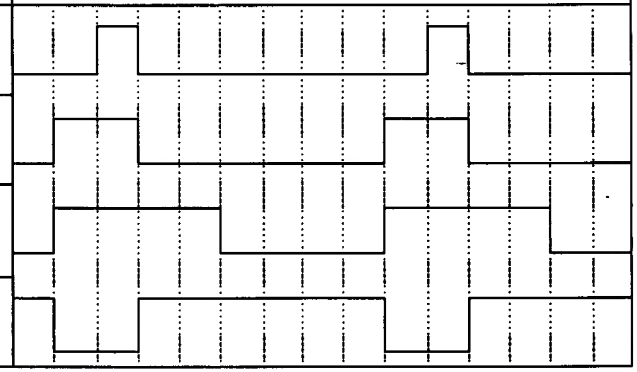


Fig. 73

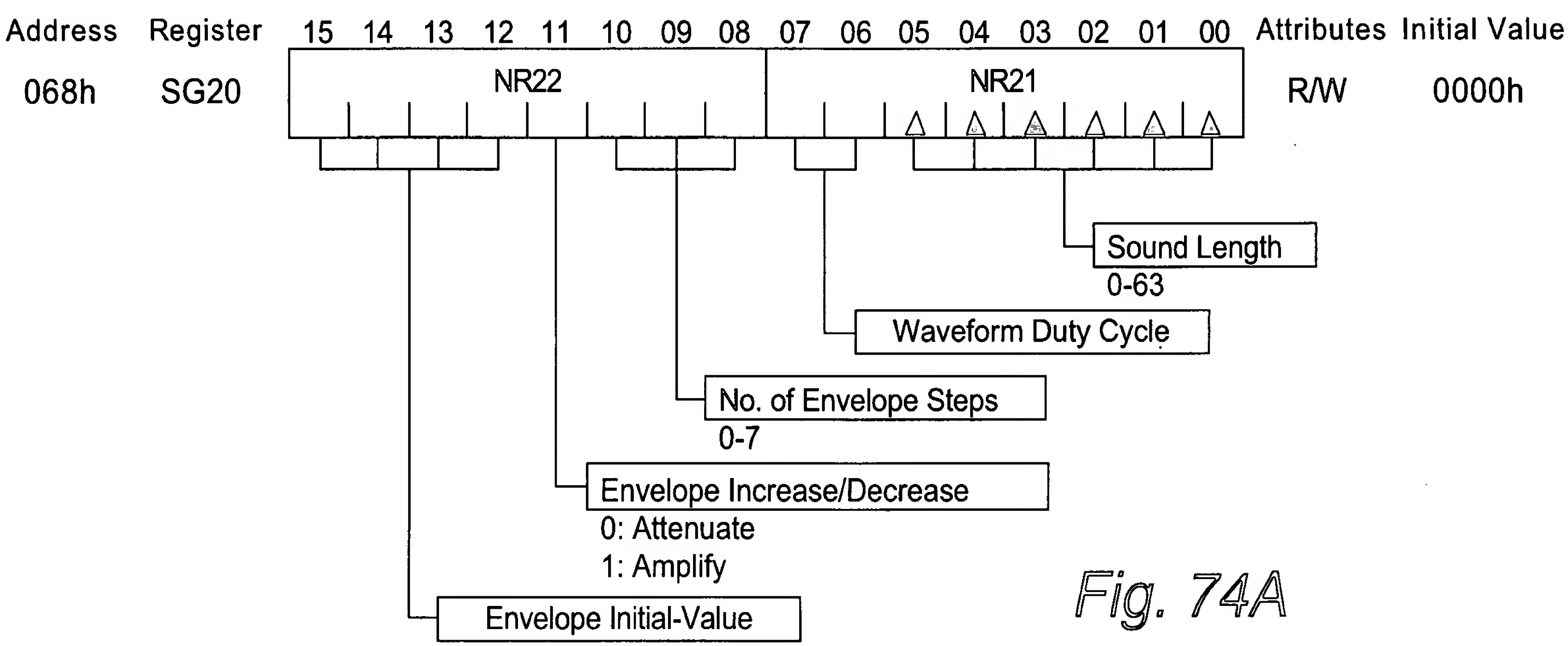


Fig. 74A

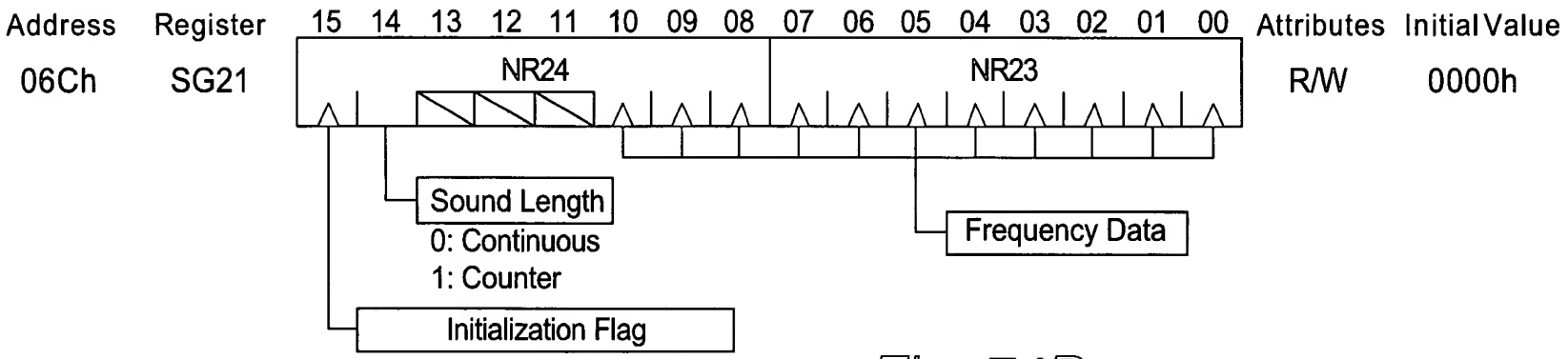


Fig. 74B

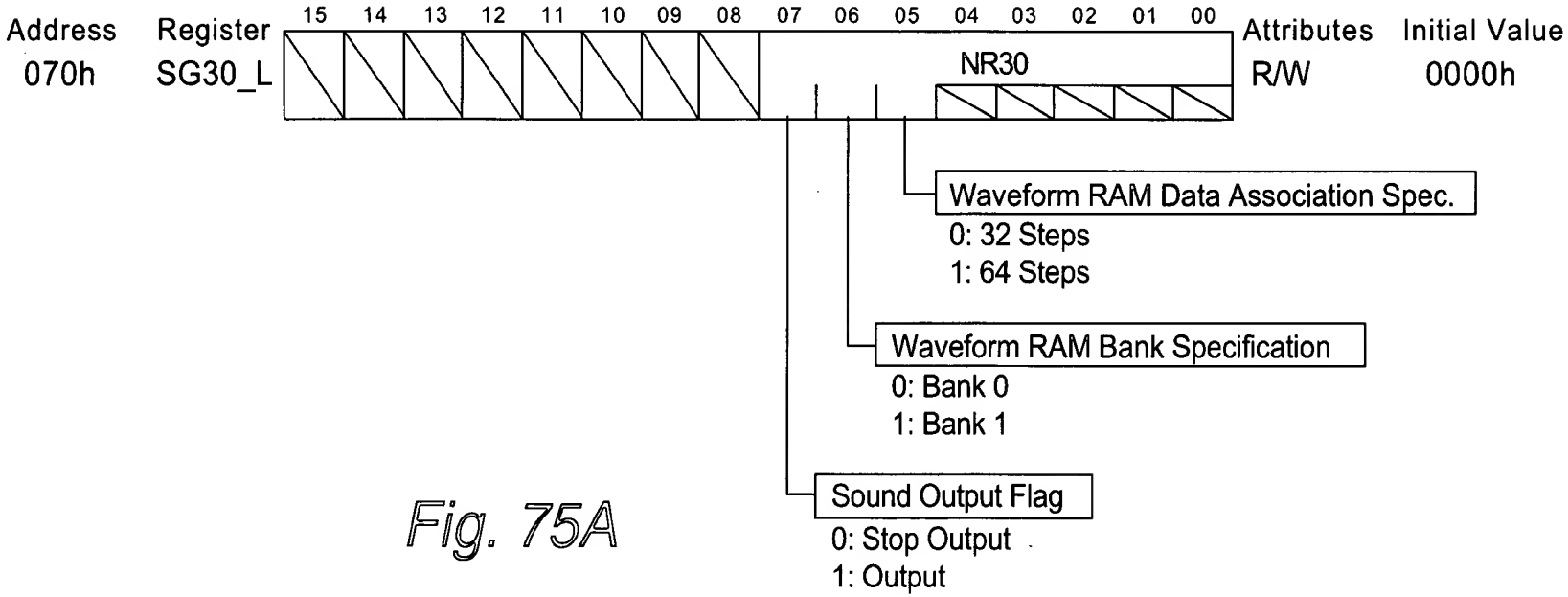


Fig. 75A

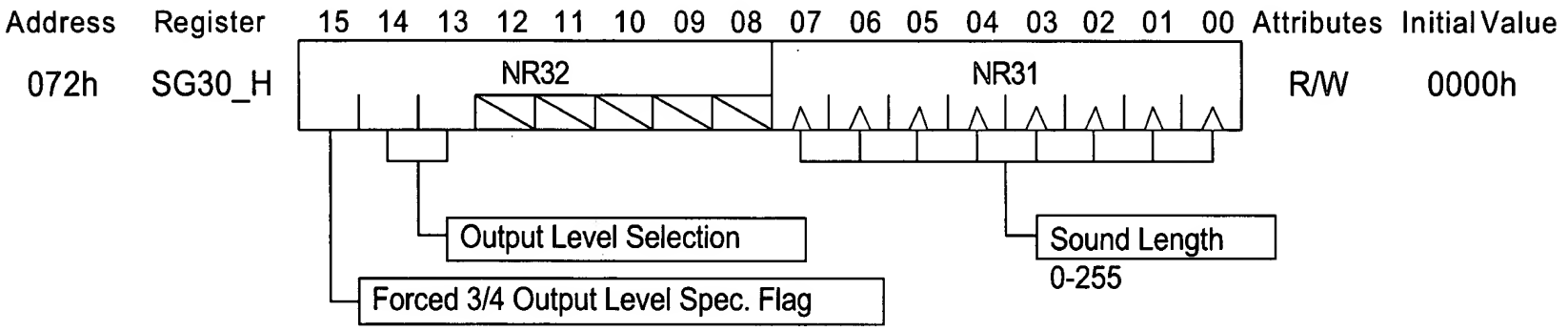


Fig. 75B

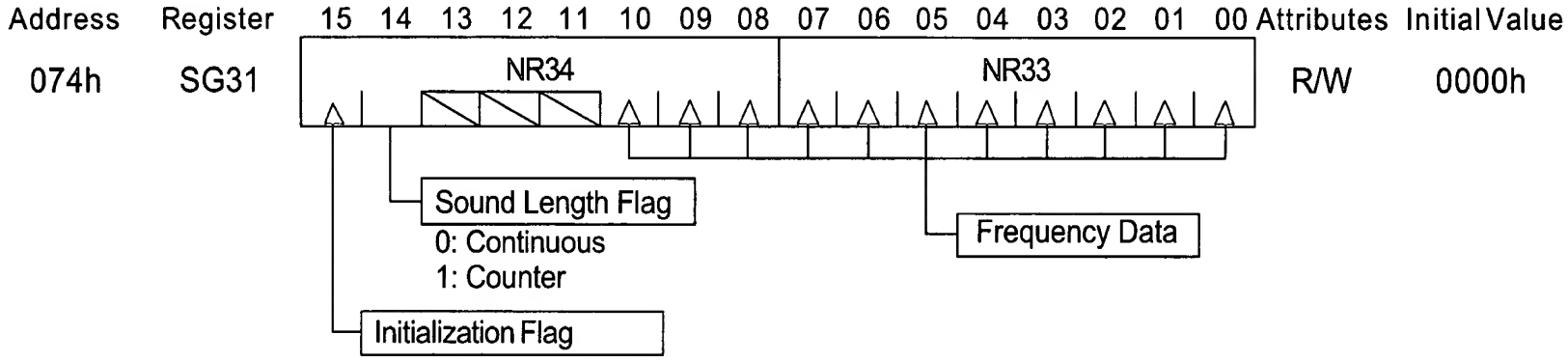


Fig. 75C

Address	Register	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00	Attributes	Initial Value
090h	SGWR0_L	Step 2	Step 3	Step 0	Step 1	R/W	-

Fig. 76A

Address	Register	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00	Attributes	Initial Value
092h	SGWR0_H	Step 6	Step 7	Step 4	Step 5	R/W	-

Fig. 76B

Address	Register	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00	Attributes	Initial Value
094h	SGWR1_L	Step 10	Step 11	Step 8	Step 9	R/W	-

Fig. 76C

Address	Register	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00	Attributes	Initial Value
096h	SGWR1_H	Step 14	Step 15	Step 12	Step 13	R/W	-

Fig. 76D

Address	Register	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00	Attributes	Initial Value
098h	SGWR2_L	Step 18	Step 19	Step 16	Step 17	R/W	-

Fig. 76E

Address	Register	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00	Attributes	Initial Value
09Ah	SGWR2_H	Step 22	Step 23	Step 20	Step 21	R/W	-

Fig. 76F

Address	Register	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00	Attributes	Initial Value
09Ch	SGWR3_L	Step 26	Step 27	Step 24	Step 25	R/W	-

Fig. 76G

Address	Register	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00	Attributes	Initial Value
09Eh	SGWR3_H	Step 30	Step 31	Step 28	Step 29	R/W	-

Fig. 76H

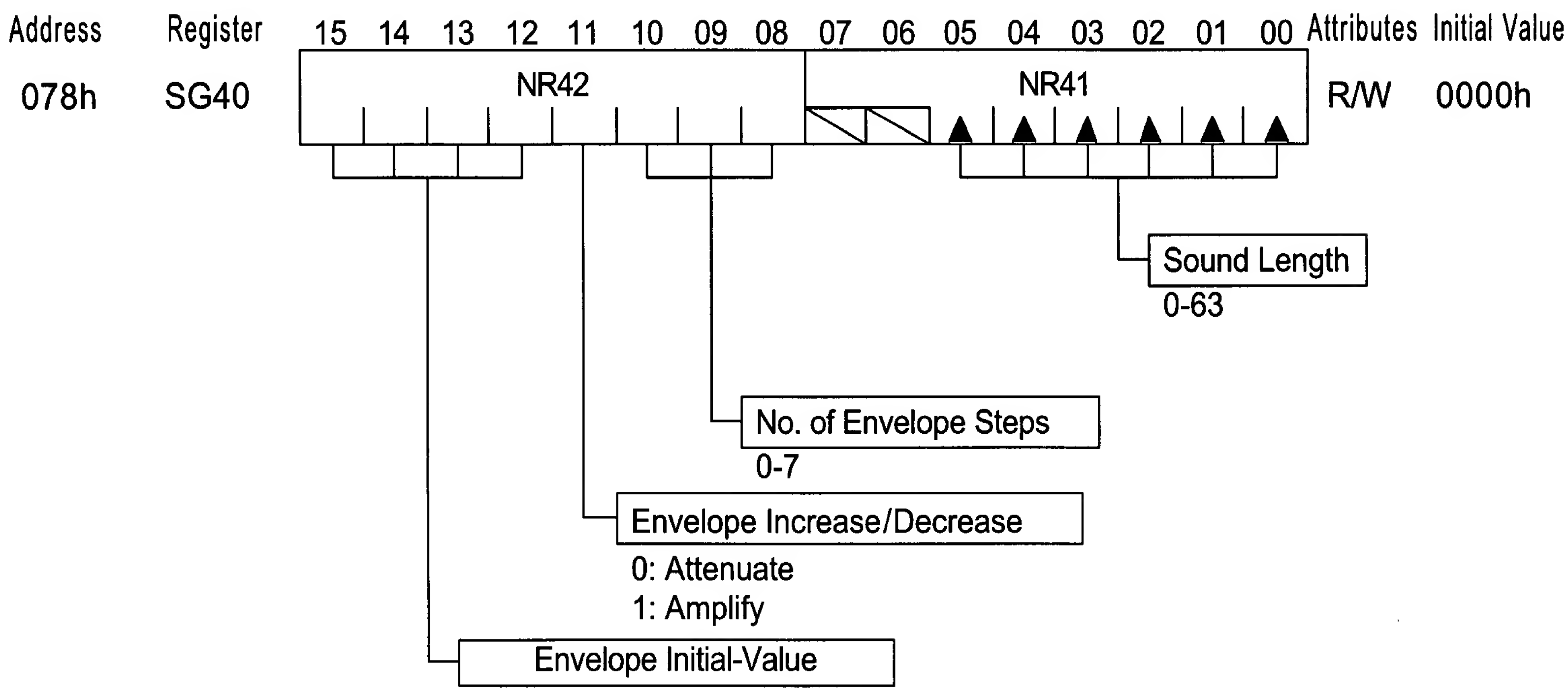

Address
078h
Register
SG40
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
NR42
NR41
Attributes
R/W
Initial Value
0000h
Sound Length
0-63
No. of Envelope Steps
0-7
Envelope Increase/Decrease
0: Attenuate
1: Amplify
Envelope Initial-Value

Fig. 77A

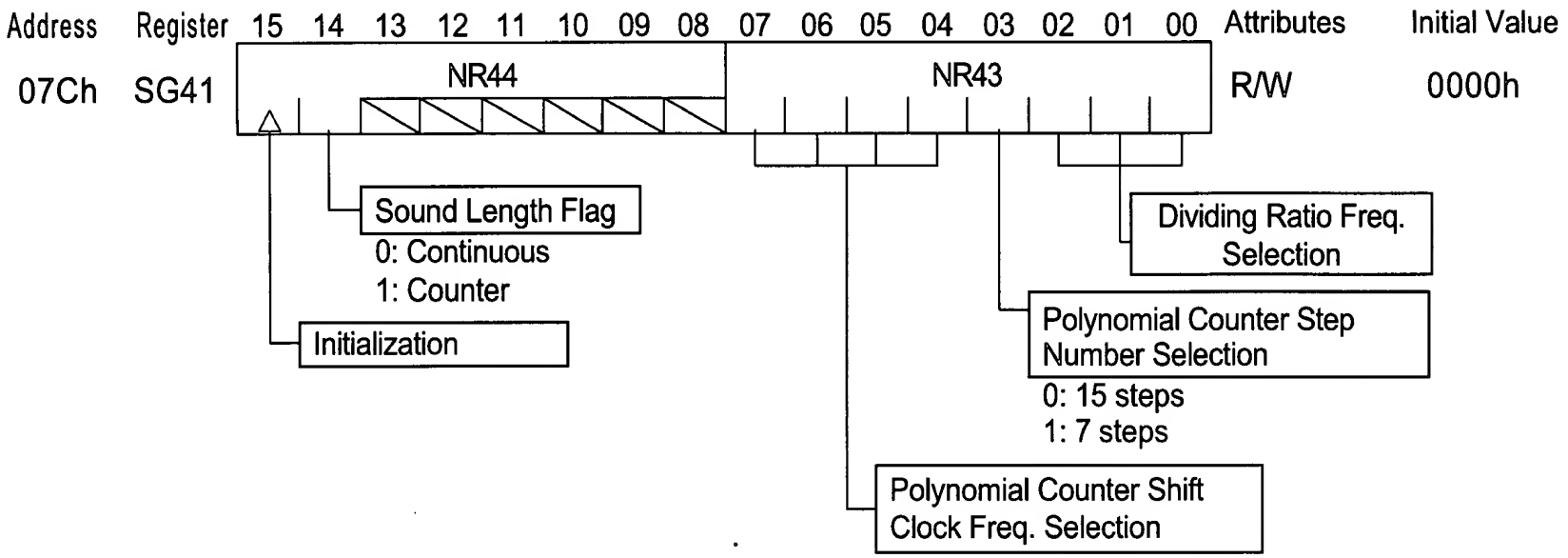

Address
Register
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Attributes
Initial Value
07Ch
SG41
NR44
NR43
R/W
0000h
Sound Length Flag
0: Continuous
1: Counter
Initialization
Dividing Ratio Freq. Selection
Polynomial Counter Step Number Selection
0: 15 steps
1: 7 steps
Polynomial Counter Shift Clock Freq. Selection

Fig. 77B

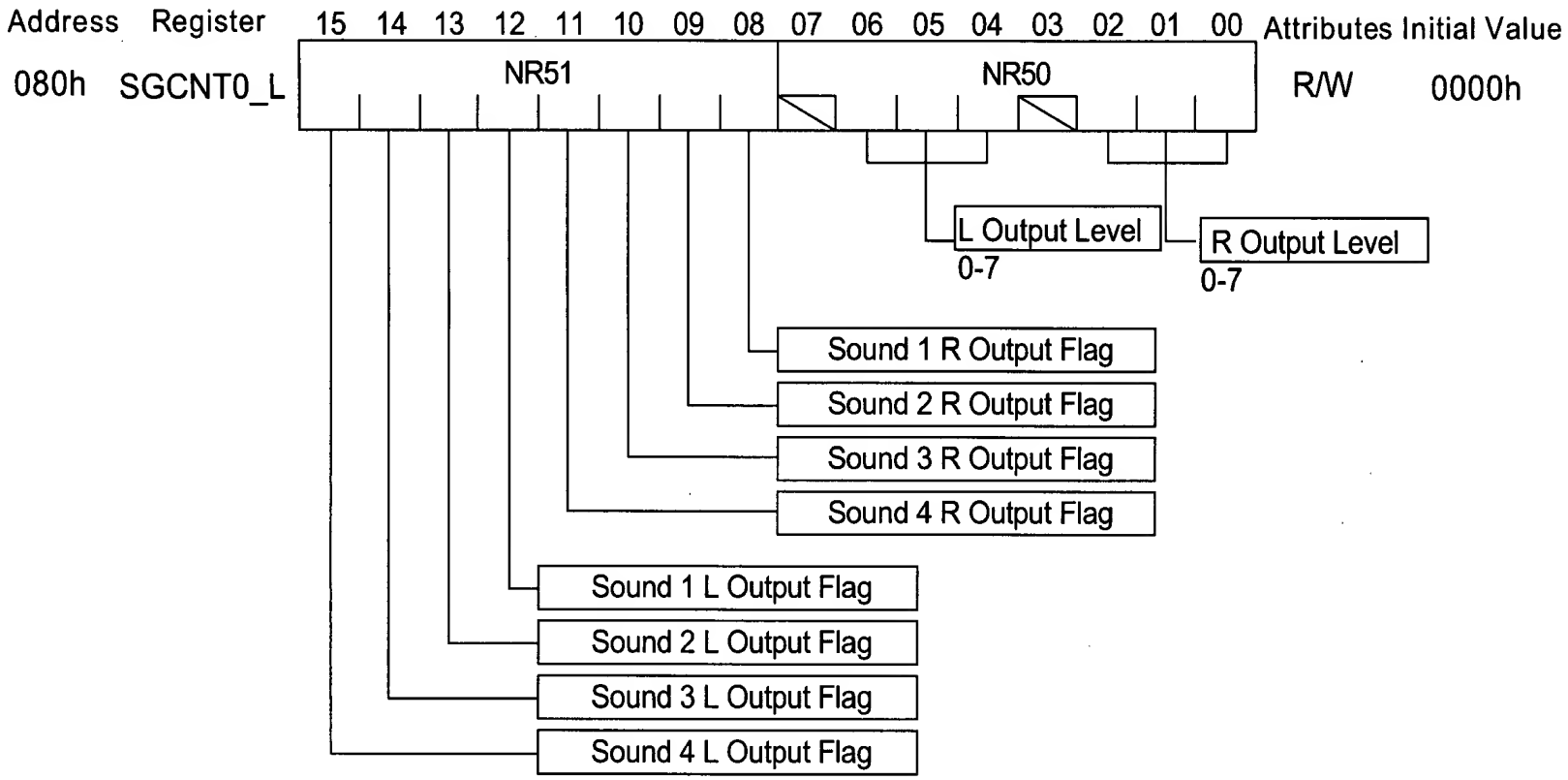

Address
Register
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Attributes
Initial Value
080h
SGCNT0_L
NR51
NR50
R/W
0000h
L Output Level
0-7
R Output Level
0-7
Sound 1 R Output Flag
Sound 2 R Output Flag
Sound 3 R Output Flag
Sound 4 R Output Flag
Sound 1 L Output Flag
Sound 2 L Output Flag
Sound 3 L Output Flag
Sound 4 L Output Flag

Fig. 78A

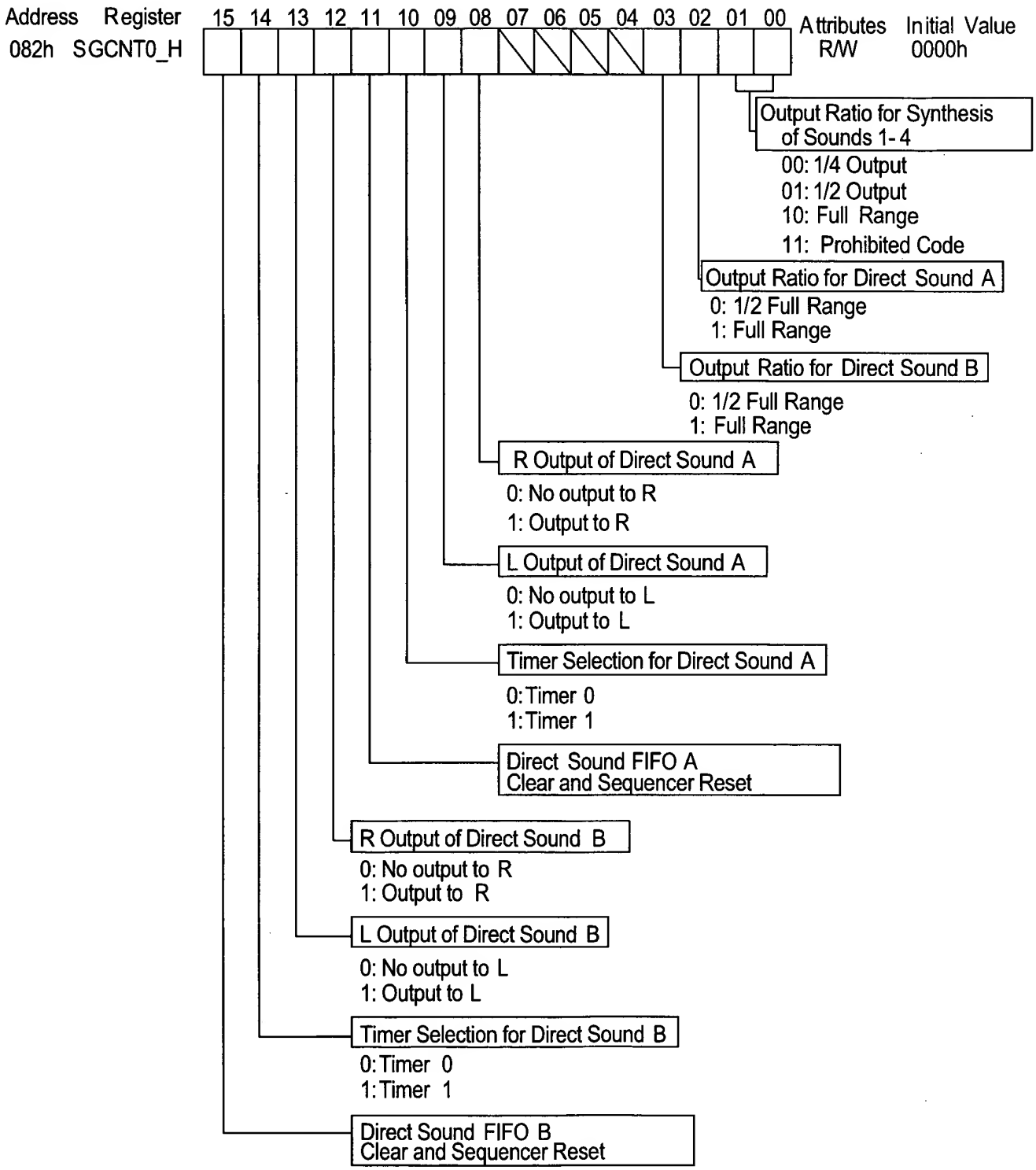

Address Register
082h SGCNT0_H
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Attributes R/W
Initial Value 0000h
Output Ratio for Synthesis of Sounds 1-4
00: 1/4 Output
01: 1/2 Output
10: Full Range
11: Prohibited Code
Output Ratio for Direct Sound A
0: 1/2 Full Range
1: Full Range
Output Ratio for Direct Sound B
0: 1/2 Full Range
1: Full Range
R Output of Direct Sound A
0: No output to R
1: Output to R
L Output of Direct Sound A
0: No output to L
1: Output to L
Timer Selection for Direct Sound A
0: Timer 0
1: Timer 1
Direct Sound FIFO A Clear and Sequencer Reset
R Output of Direct Sound B
0: No output to R
1: Output to R
L Output of Direct Sound B
0: No output to L
1: Output to L
Timer Selection for Direct Sound B
0: Timer 0
1: Timer 1
Direct Sound FIFO B Clear and Sequencer Reset

Fig. 78B

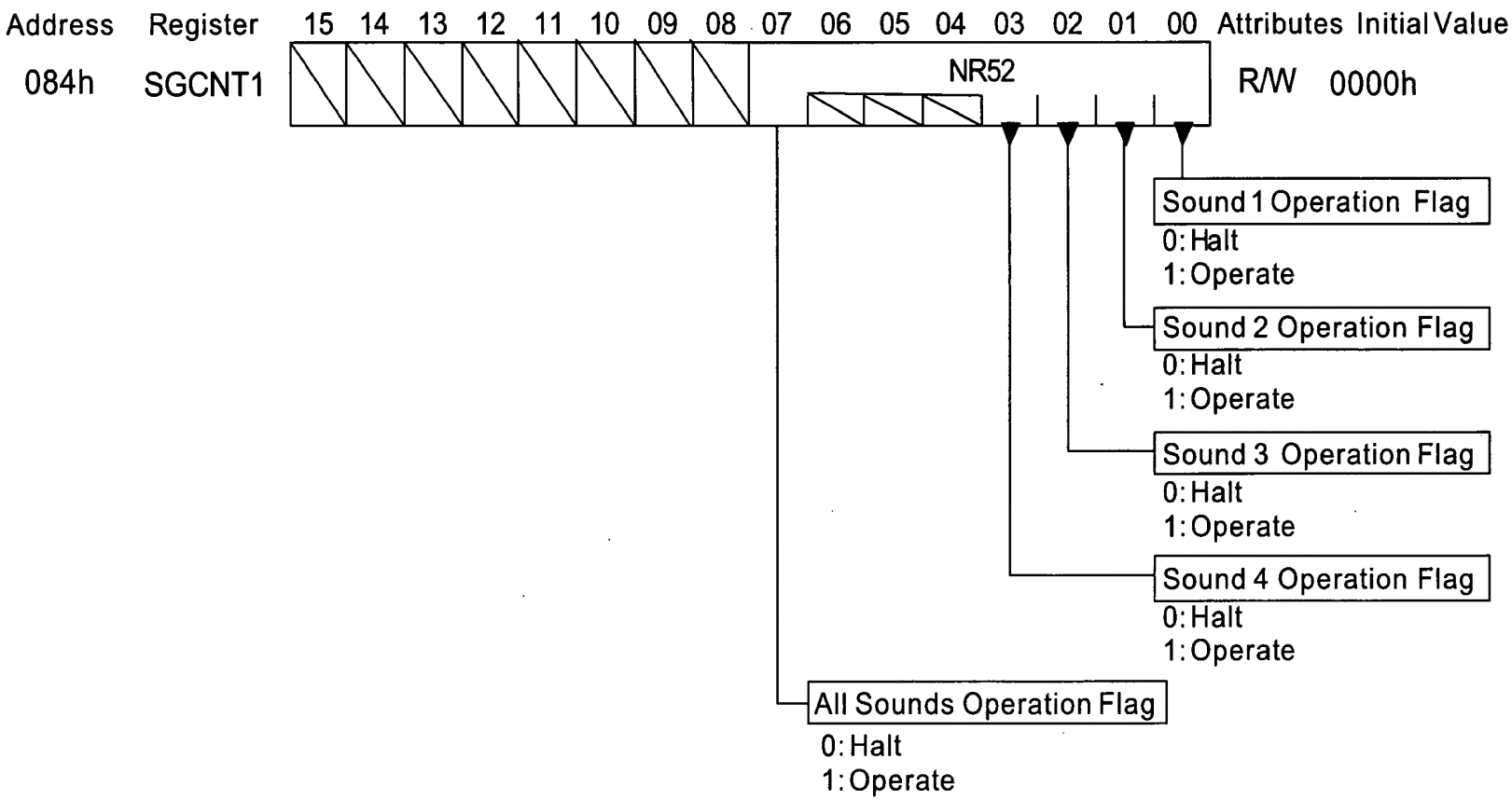


Fig. 78C

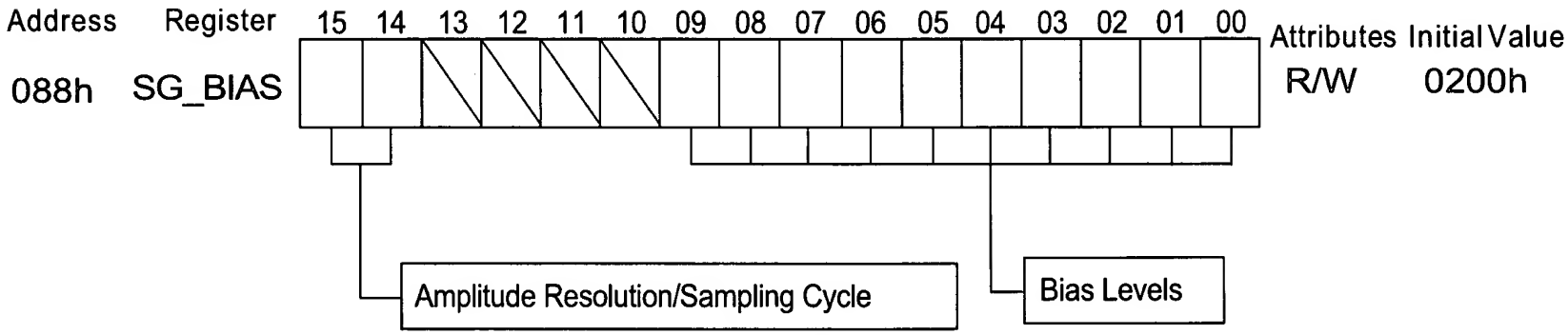


Fig. 79

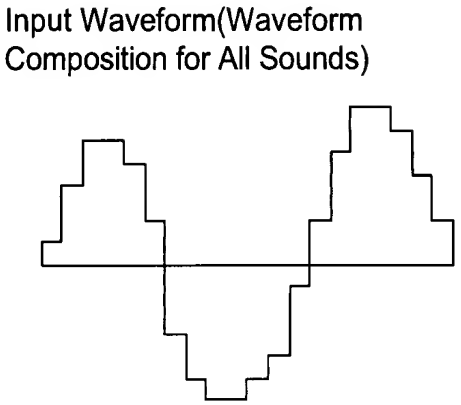


Fig. 80A

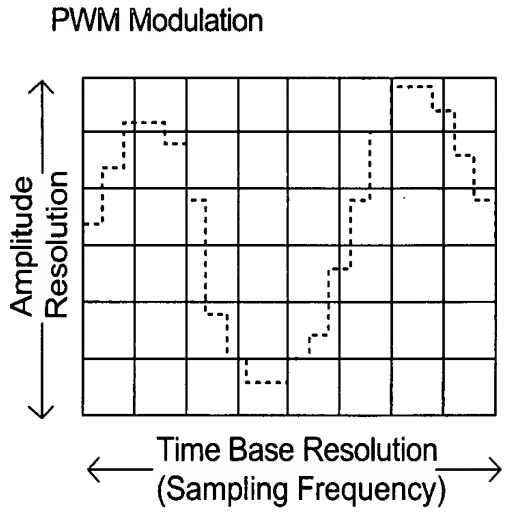


Fig. 80B

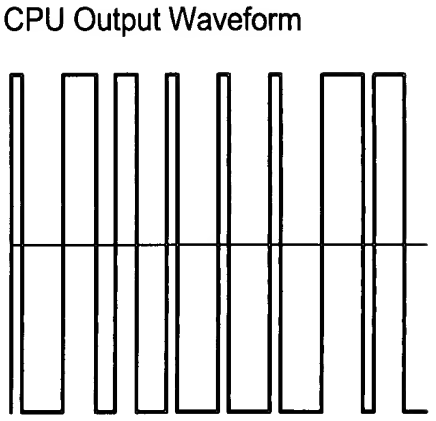


Fig. 80C

1) Timer Setting

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
100h	TM0D																	R/W	0000h
104h	TM1D																		
108h	TM2D																		
10Ch	TM3D																		

Fig. 81A

2) Timer Control

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
102h	TM0CNT																	R/W	0000h
106h	TM1CNT																		
10Ah	TM2CNT																		
10Eh	TM3CNT																		

Prescalar Selection

Count-up Timing

Interrupt Request Enable Flag
0: Disable
1: Enable

Timer Operation Flag
0: Disable
1: Enable

Fig. 81B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0B0h	DM0SAD_L																	W	0000h

Fig. 82A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0B2h	DM0SAD_H	\	\	\	\	\												W	0000h

Fig. 82B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0B4h	DM0DAD_L																	W	0000h

Fig. 83A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0B6h	DM0DAD_H	\	\	\	\	\												W	0000h

Fig. 83B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0B8h	DM0CNT_L	\	\															W	0000h

Fig. 84

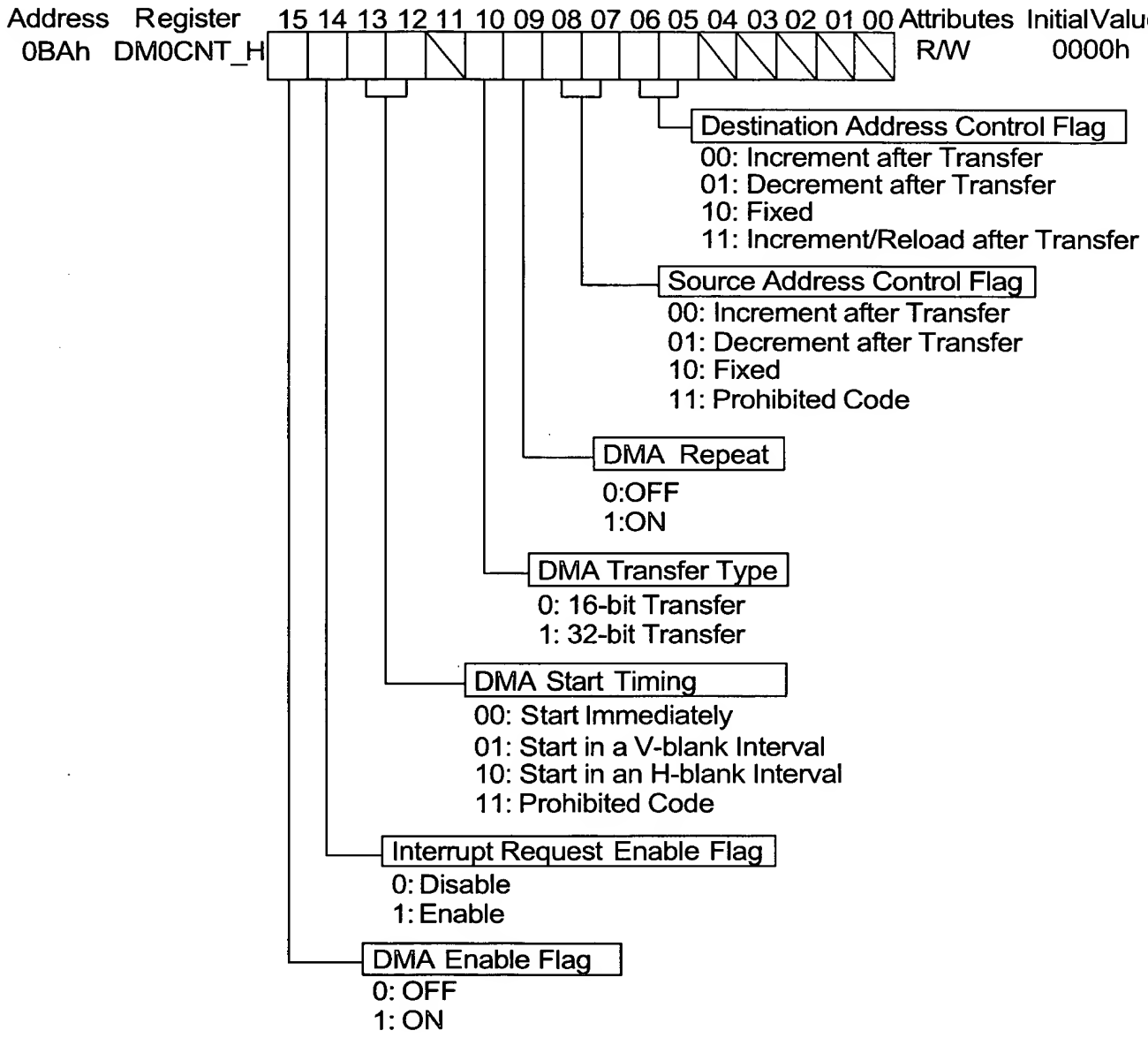

Address Register 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes InitialValue
0BAh DM0CNT_H R/W 0000h
Destination Address Control Flag
00: Increment after Transfer
01: Decrement after Transfer
10: Fixed
11: Increment/Reload after Transfer
Source Address Control Flag
00: Increment after Transfer
01: Decrement after Transfer
10: Fixed
11: Prohibited Code
DMA Repeat
0:OFF
1:ON
DMA Transfer Type
0: 16-bit Transfer
1: 32-bit Transfer
DMA Start Timing
00: Start Immediately
01: Start in a V-blank Interval
10: Start in an H-blank Interval
11: Prohibited Code
Interrupt Request Enable Flag
0: Disable
1: Enable
DMA Enable Flag
0: OFF
1: ON

Fig. 85

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0BCh	DM1SAD_L																	W	0000h
0C8h	DM2SAD_L																		

Fig. 86A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0BEh	DM1SAD_H	\	\	\	\													W	0000h
0CAh	DM2SAD_H																		

Fig. 86B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0C0h	DM1DAD_L																	W	0000h
0CCh	DM2DAD_L																		

Fig. 87A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0C2h	DM1DAD_H	\	\	\	\	\												W	0000h
0CEh	DM2DAD_H																		

Fig. 87B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0C4h	DM1CNT_L	\	\															W	0000h
0D0h	DM2CNT_L																		

Fig. 88

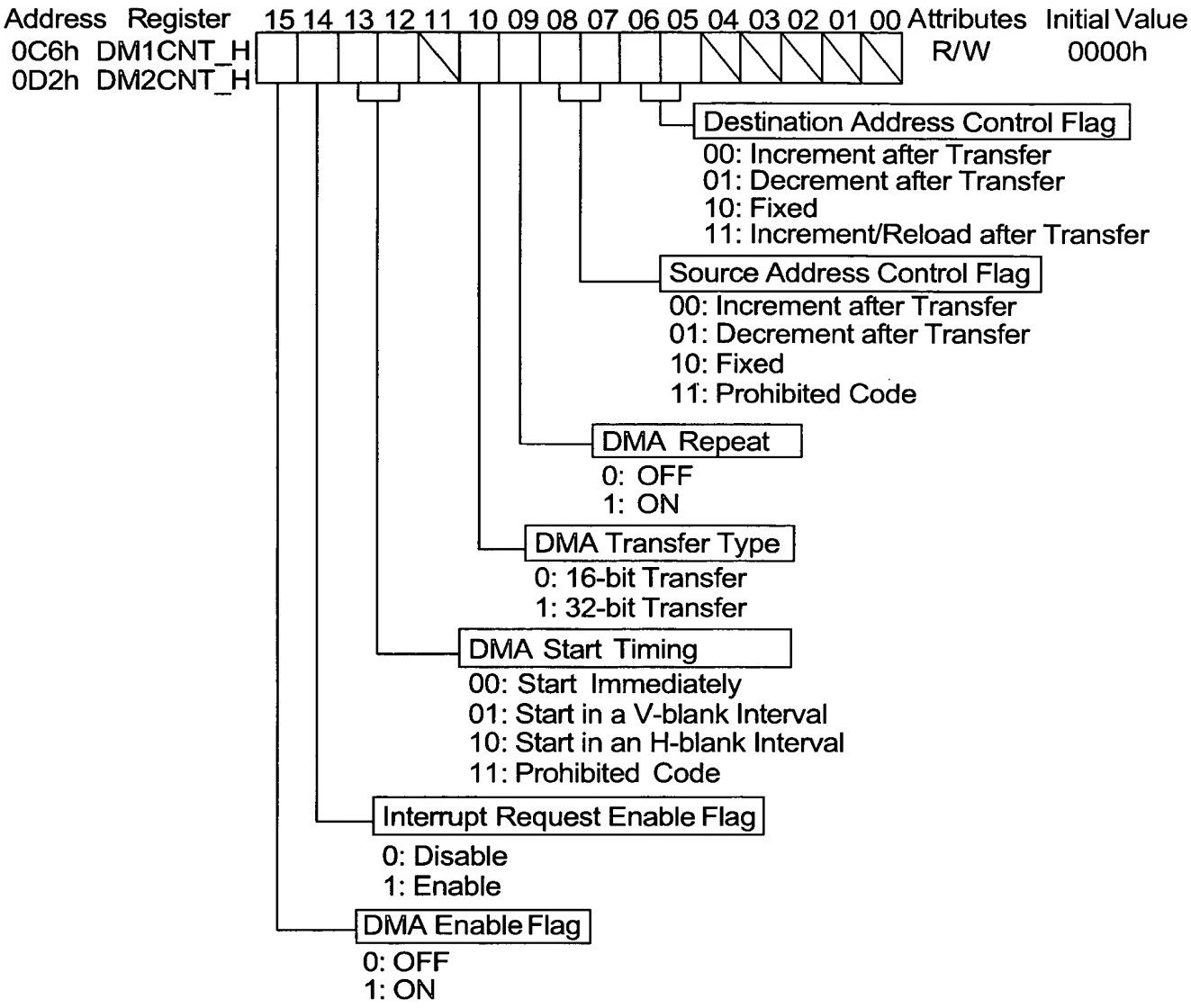

Address Register 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes Initial Value
0C6h DM1CNT_H
0D2h DM2CNT_H
R/W 0000h
Destination Address Control Flag
00: Increment after Transfer
01: Decrement after Transfer
10: Fixed
11: Increment/Reload after Transfer
Source Address Control Flag
00: Increment after Transfer
01: Decrement after Transfer
10: Fixed
11: Prohibited Code
DMA Repeat
0: OFF
1: ON
DMA Transfer Type
0: 16-bit Transfer
1: 32-bit Transfer
DMA Start Timing
00: Start Immediately
01: Start in a V-blank Interval
10: Start in an H-blank Interval
11: Prohibited Code
Interrupt Request Enable Flag
0: Disable
1: Enable
DMA Enable Flag
0: OFF
1: ON

Fig. 89

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0D4h	DM3SAD_L																	W	0000h

Fig. 90A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0D6h	DM3SAD_H	\	\	\	\													W	0000h

Fig. 90B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0D8h	DM3DAD_L																	W	0000h

Fig. 91A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0DAh	DM3DAD_H	\	\	\	\													W	0000h

Fig. 91B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0DCh	DM3CNT_L																	W	0000h

Fig. 92

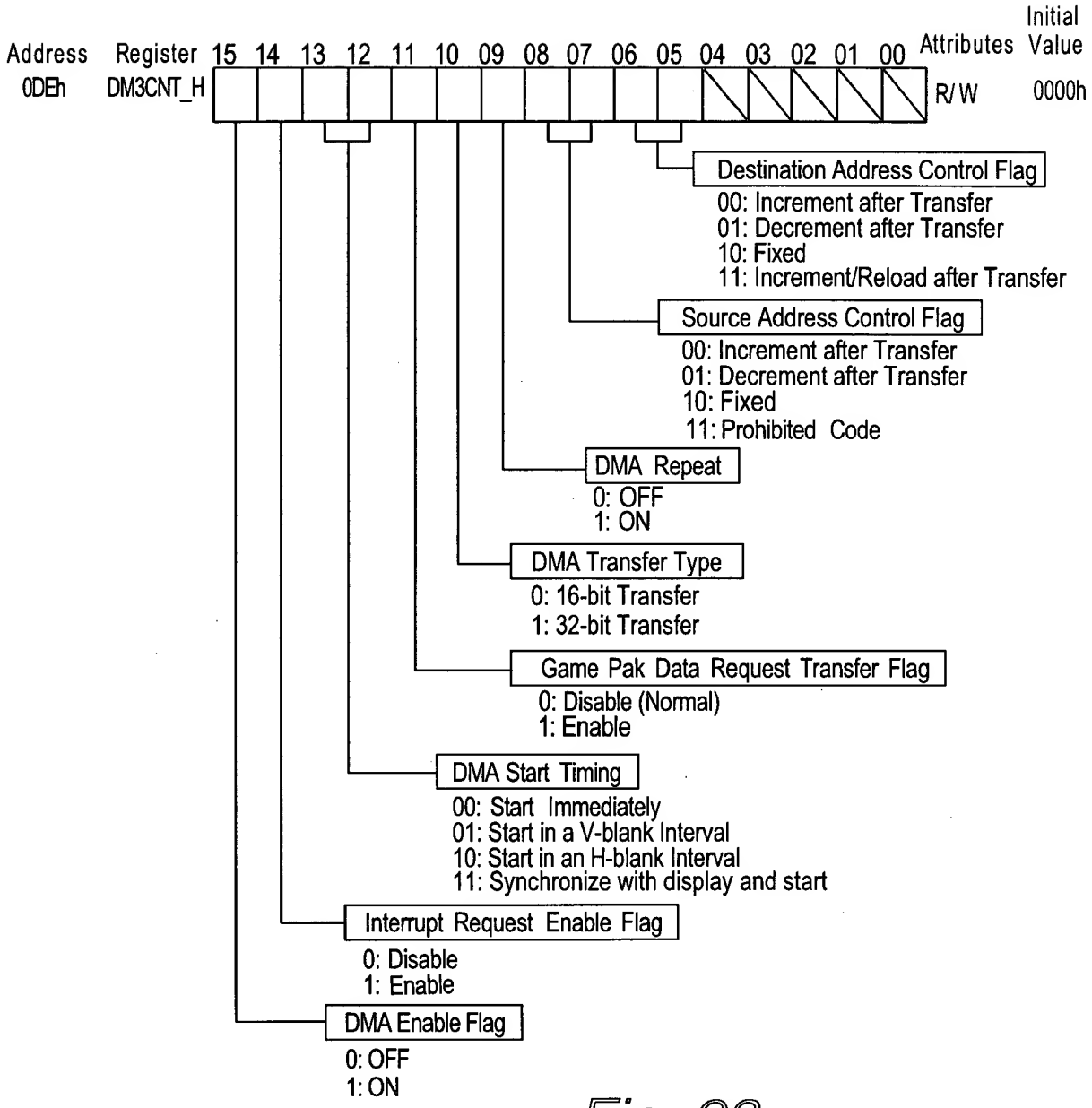

Address
Register
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Attributes
Initial Value
0DEh
DM3CNT_H
R/W
0000h
Destination Address Control Flag
00: Increment after Transfer
01: Decrement after Transfer
10: Fixed
11: Increment/Reload after Transfer
Source Address Control Flag
00: Increment after Transfer
01: Decrement after Transfer
10: Fixed
11: Prohibited Code
DMA Repeat
0: OFF
1: ON
DMA Transfer Type
0: 16-bit Transfer
1: 32-bit Transfer
Game Pak Data Request Transfer Flag
0: Disable (Normal)
1: Enable
DMA Start Timing
00: Start Immediately
01: Start in a V-blank Interval
10: Start in an H-blank Interval
11: Synchronize with display and start
Interrupt Request Enable Flag
0: Disable
1: Enable
DMA Enable Flag
0: OFF
1: ON

Fig. 93

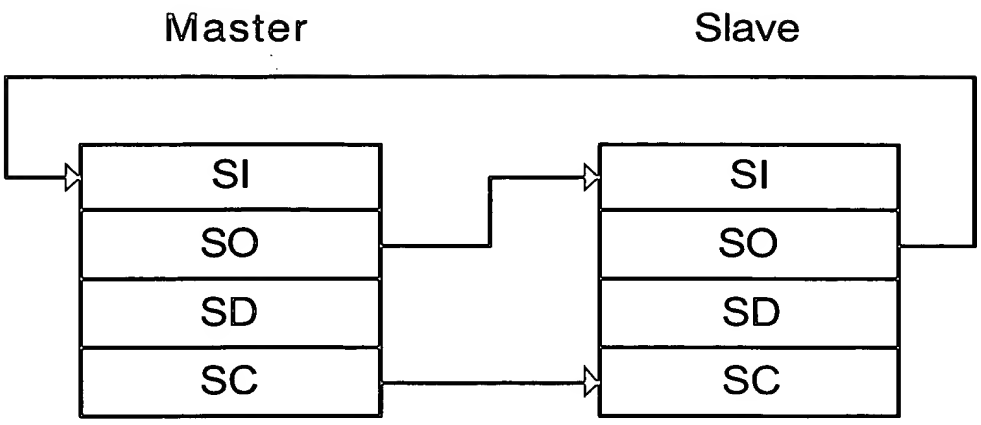


Fig. 94

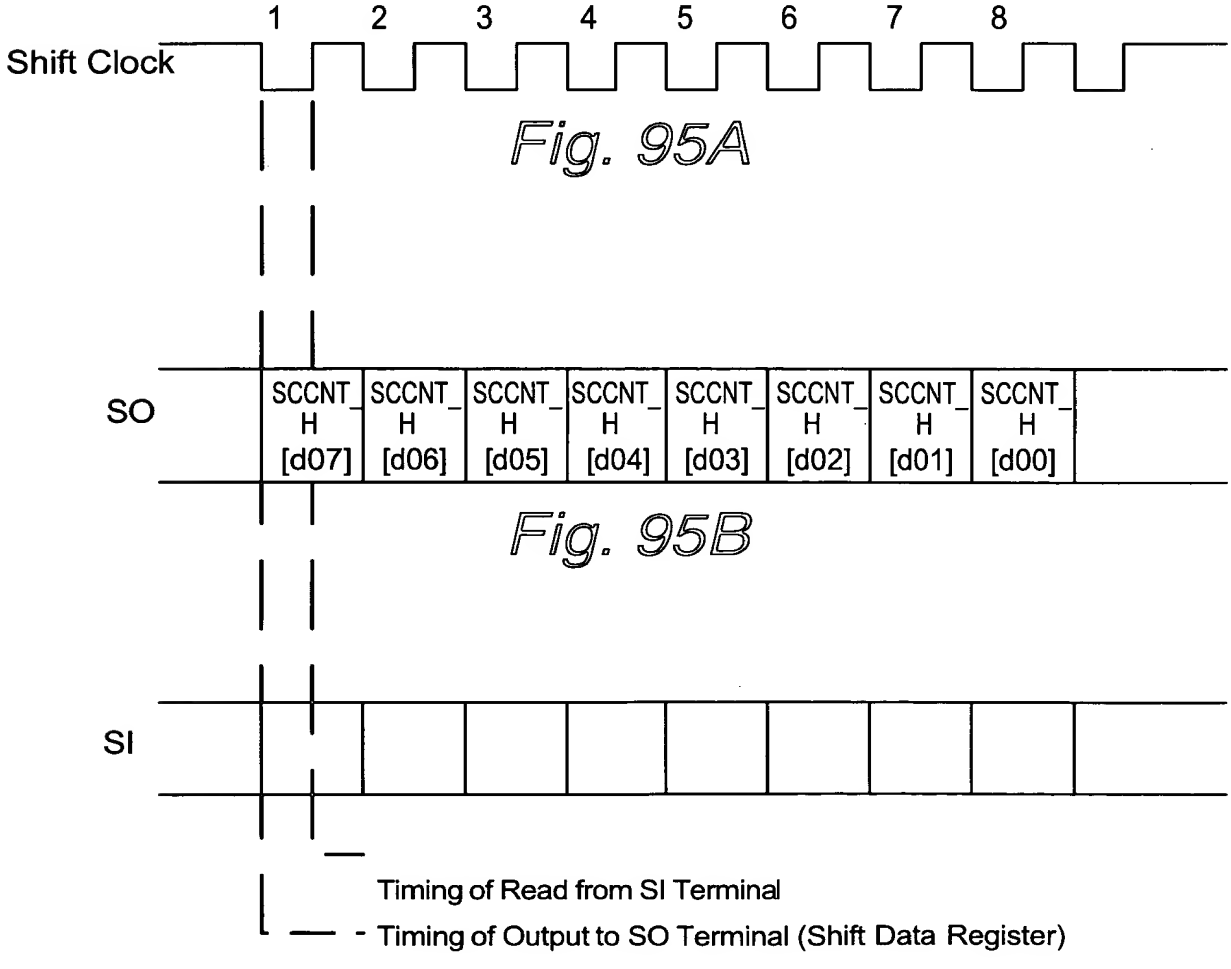


Fig. 95A

Fig. 95B

Fig. 95C

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
12A h	SCCNT_H																	R/W	0000h

Fig. 96

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
120h	SCD0	Data 0																R/W	0000h

Fig. 97A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
122h	SCD1	Data 1																R/W	0000h

Fig. 97B

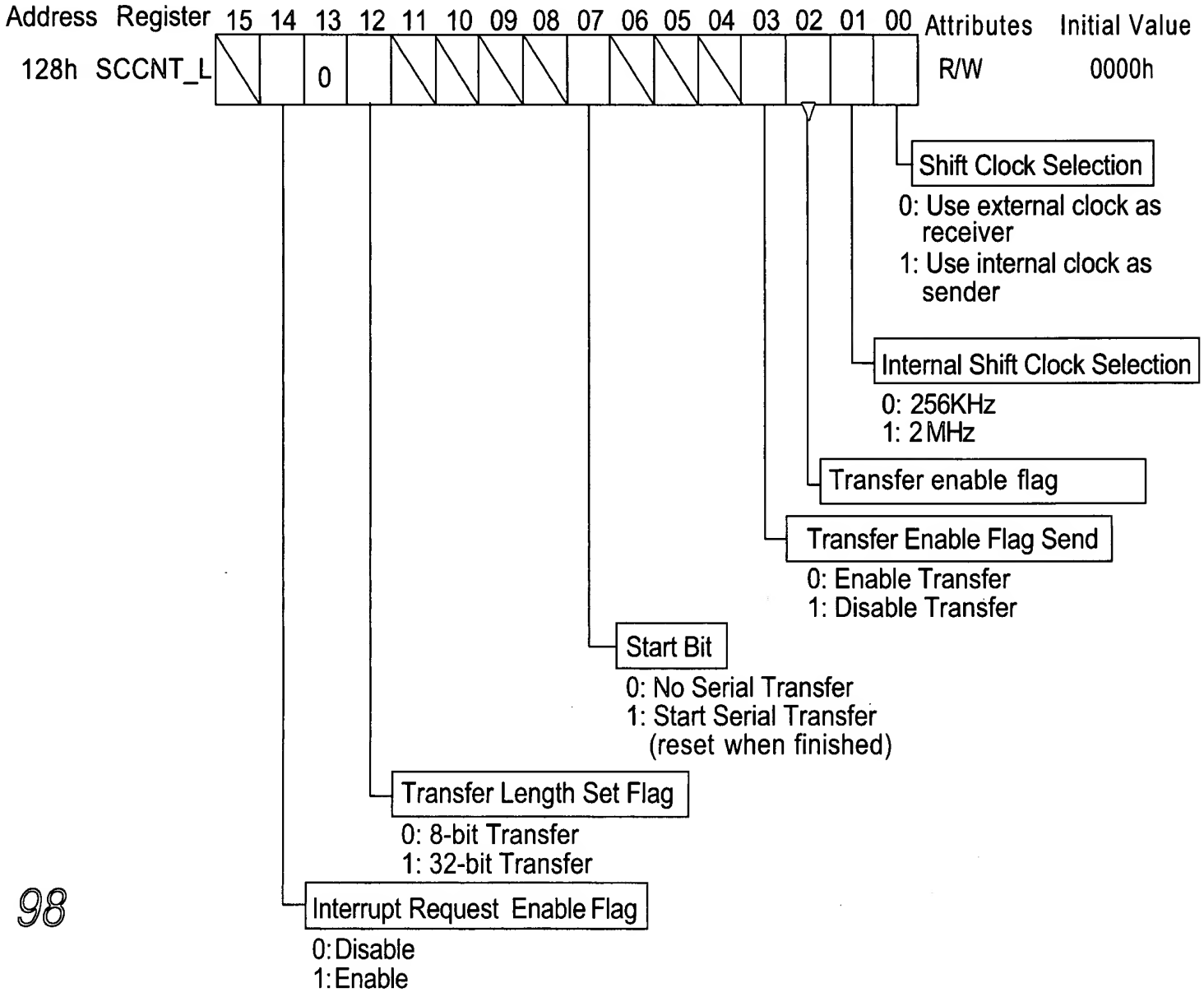
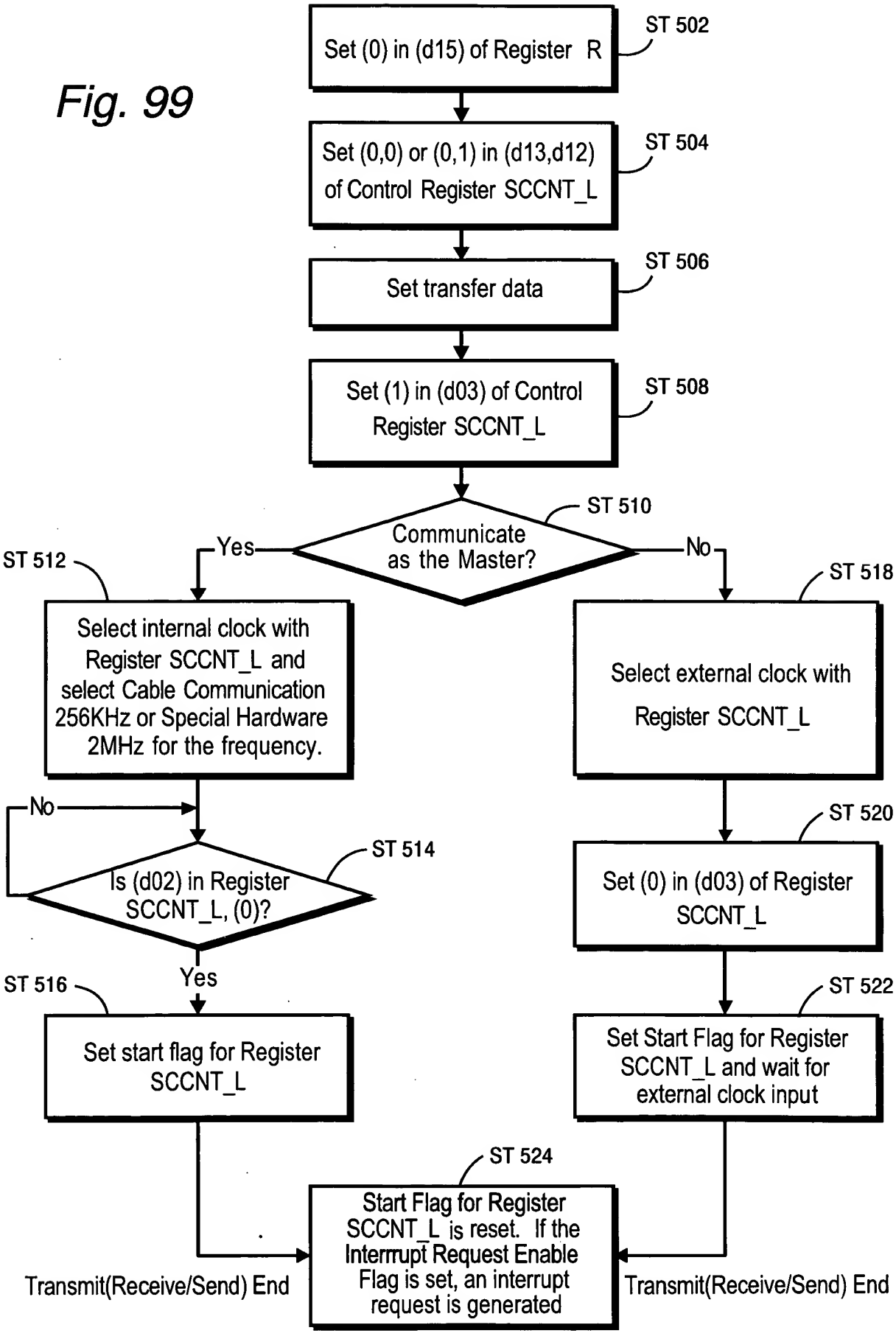

Address Register
128h SCCNT_L
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
0
Attributes
R/W
Initial Value
0000h
Shift Clock Selection
0: Use external clock as receiver
1: Use internal clock as sender
Internal Shift Clock Selection
0: 256KHz
1: 2MHz
Transfer enable flag
Transfer Enable Flag Send
0: Enable Transfer
1: Disable Transfer
Start Bit
0: No Serial Transfer
1: Start Serial Transfer
(reset when finished)
Transfer Length Set Flag
0: 8-bit Transfer
1: 32-bit Transfer
Interrupt Request Enable Flag
0: Disable
1: Enable

Fig. 98

Fig. 99


Set (0) in (d15) of Register R
ST 502
Set (0,0) or (0,1) in (d13,d12) of Control Register SCCNT_L
ST 504
Set transfer data
ST 506
Set (1) in (d03) of Control Register SCCNT_L
ST 508
Communicate as the Master?
ST 510
Yes
No
ST 512
Select internal clock with Register SCCNT_L and select Cable Communication 256KHz or Special Hardware 2MHz for the frequency.
ST 518
Select external clock with Register SCCNT_L
No
Is (d02) in Register SCCNT_L, (0)?
ST 514
ST 520
Set (0) in (d03) of Register SCCNT_L
Yes
ST 516
Set start flag for Register SCCNT_L
ST 522
Set Start Flag for Register SCCNT_L and wait for external clock input
ST 524
Start Flag for Register SCCNT_L is reset. If the Interrupt Request Enable Flag is set, an interrupt request is generated
Transmit(Receive/Send) End
Transmit(Receive/Send) End

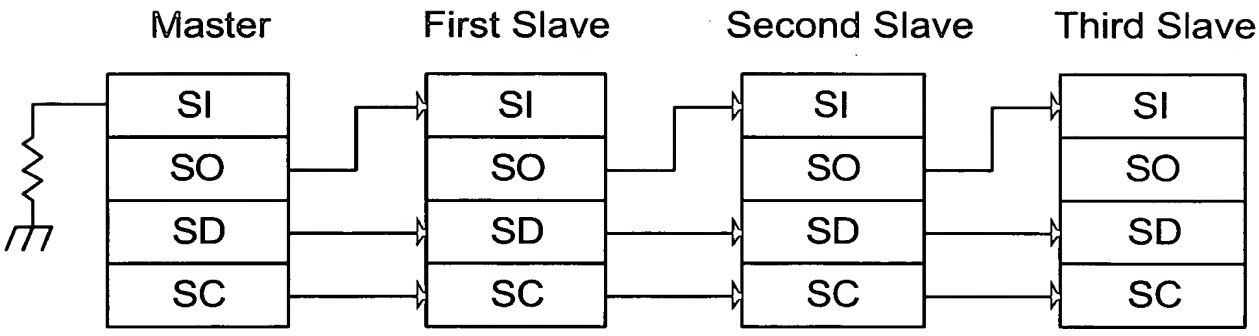

Master
First Slave
Second Slave
Third Slave
SI
SO
SD
SC
SI
SO
SD
SC
SI
SO
SD
SC
SI
SO
SD
SC

Fig. 100

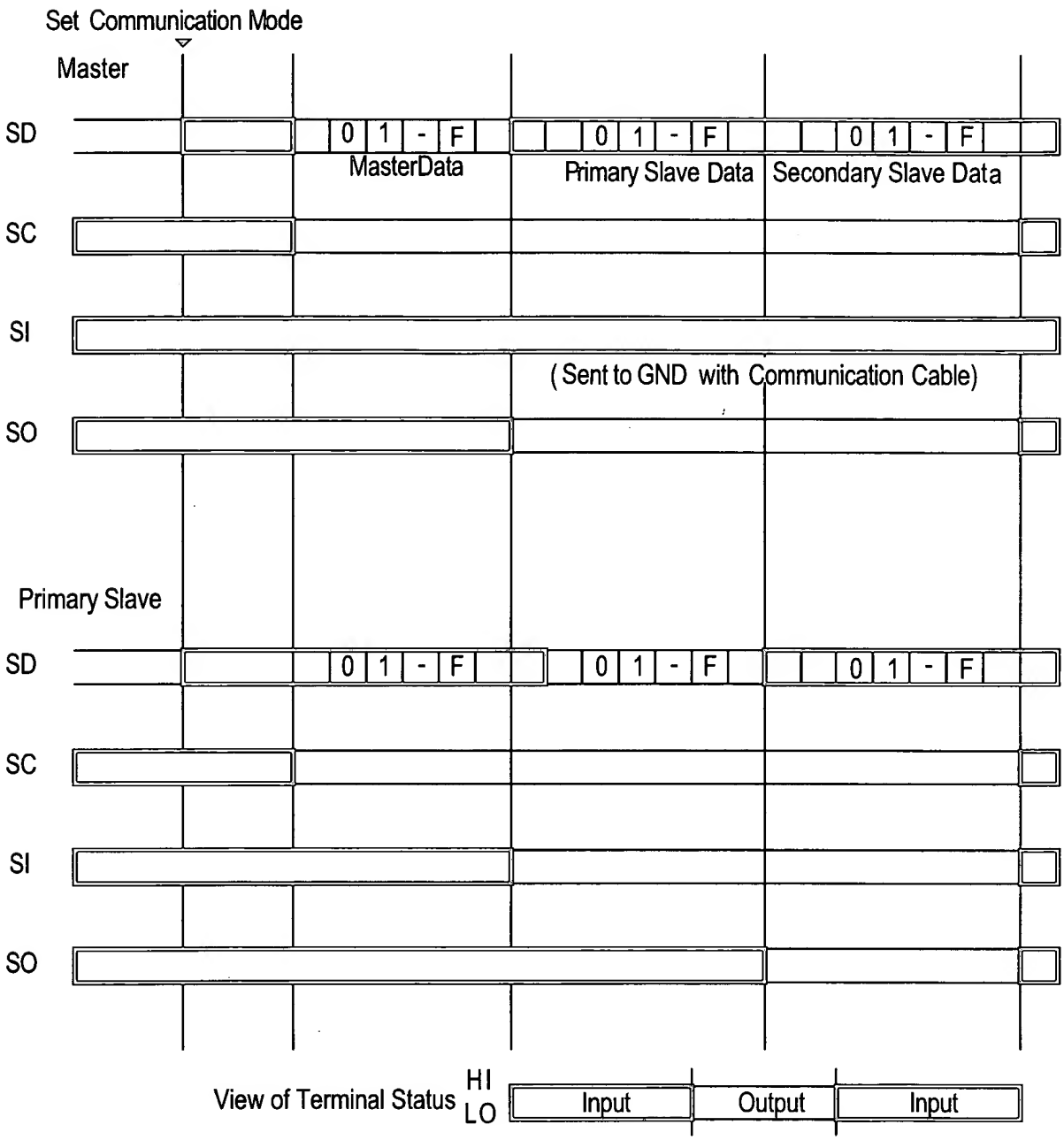


Fig. 101

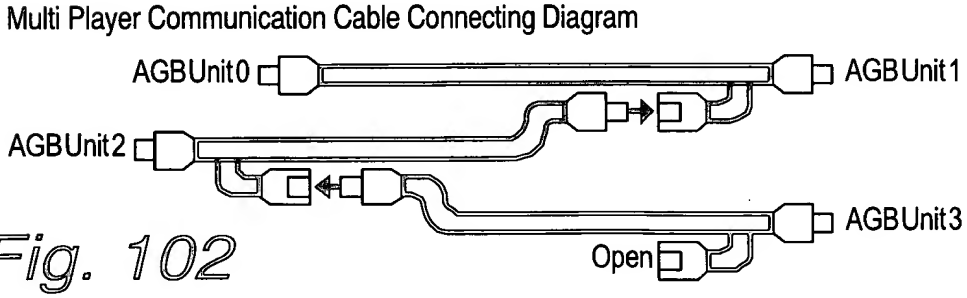


Fig. 102

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
12Ah	SCCNT_H																	R/W	0000h

Fig.103

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
120h	SCD0	Data 0																R/W	0000h

Fig. 104A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
122h	SCD1	Data 1																R/W	0000h

Fig. 104B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
124h	SCD2	Data 2																R/W	0000h

Fig. 104C

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
126h	SCD3	Data 3																R/W	0000h

Fig. 104D

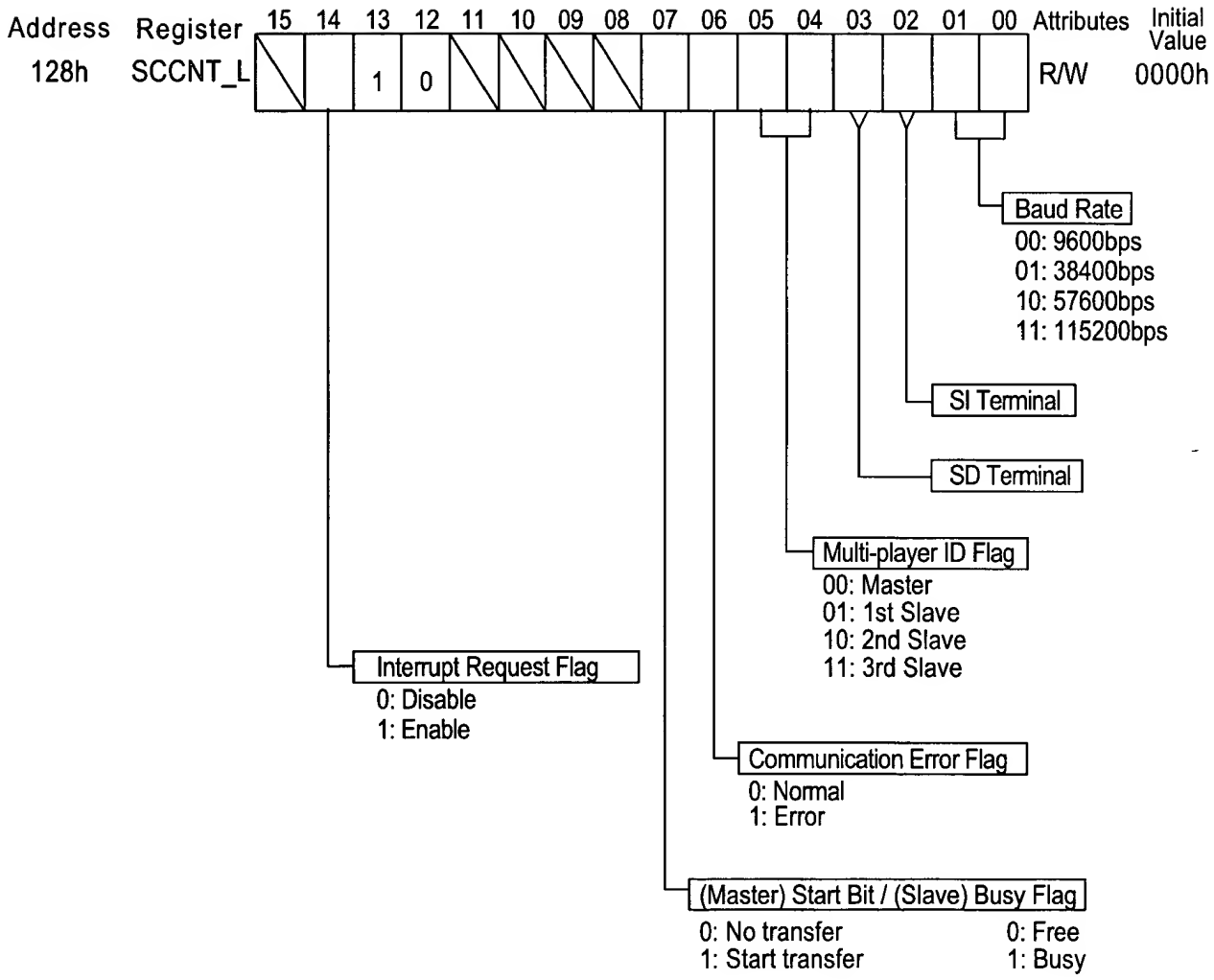

Address
128h
Register
SCCNT_L
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
1
0
Attributes
R/W
Initial Value
0000h
Baud Rate
00: 9600bps
01: 38400bps
10: 57600bps
11: 115200bps
SI Terminal
SD Terminal
Multi-player ID Flag
00: Master
01: 1st Slave
10: 2nd Slave
11: 3rd Slave
Interrupt Request Flag
0: Disable
1: Enable
Communication Error Flag
0: Normal
1: Error
(Master) Start Bit / (Slave) Busy Flag
0: No transfer
1: Start transfer
0: Free
1: Busy

Fig. 105

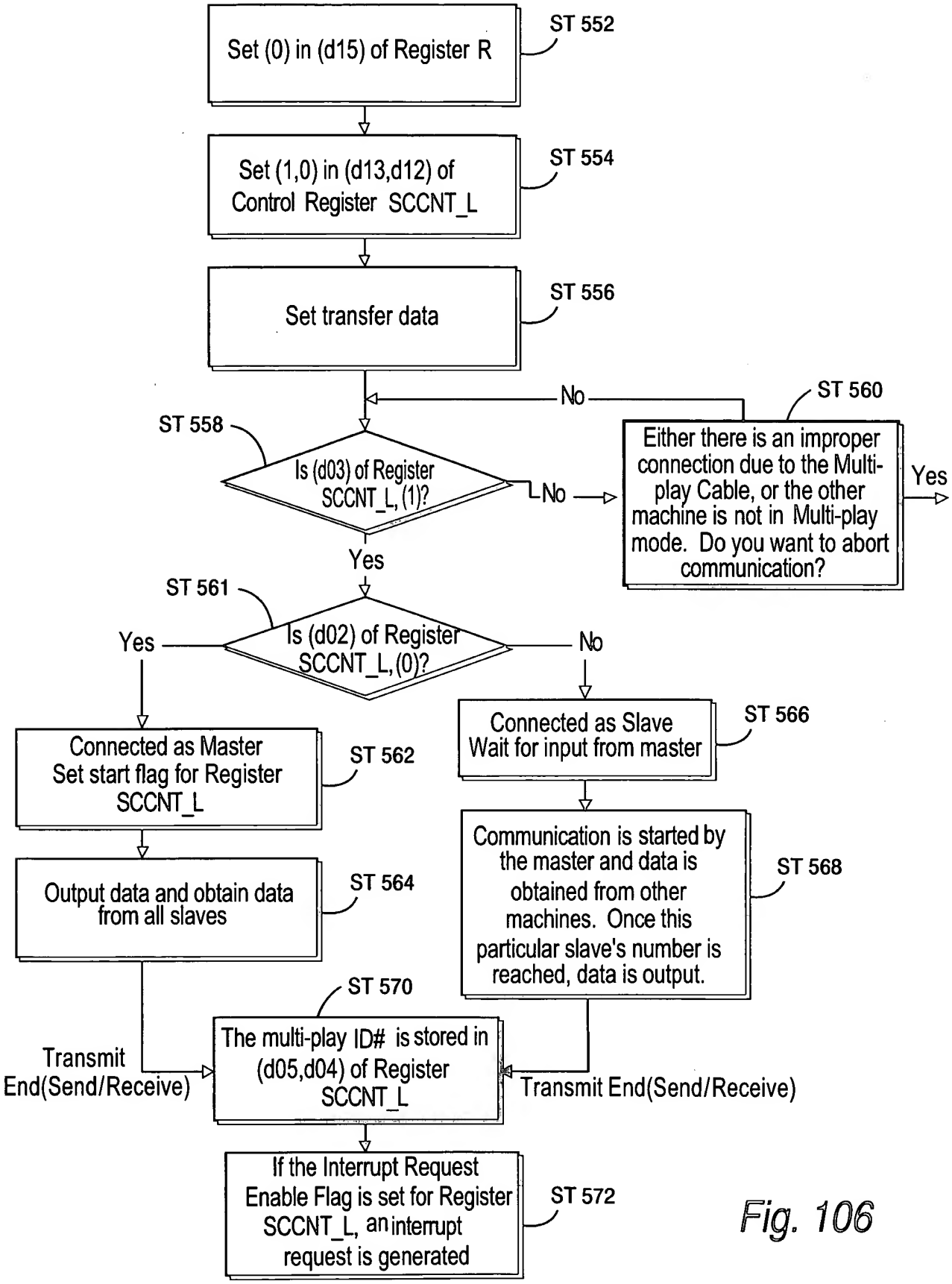

Set (0) in (d15) of Register R
ST 552
Set (1,0) in (d13,d12) of Control Register SCCNT_L
ST 554
Set transfer data
ST 556
No
ST 560
ST 558
Is (d03) of Register SCCNT_L, (1)?
No
Either there is an improper connection due to the Multi-play Cable, or the other machine is not in Multi-play mode. Do you want to abort communication?
Yes
Yes
ST 561
Is (d02) of Register SCCNT_L, (0)?
Yes
No
Connected as Master Set start flag for Register SCCNT_L
ST 562
Connected as Slave Wait for input from master
ST 566
Output data and obtain data from all slaves
ST 564
Communication is started by the master and data is obtained from other machines. Once this particular slave's number is reached, data is output.
ST 568
ST 570
Transmit End(Send/Receive)
The multi-play ID# is stored in (d05,d04) of Register SCCNT_L
Transmit End(Send/Receive)
If the Interrupt Request Enable Flag is set for Register SCCNT_L, an interrupt request is generated
ST 572

Fig. 106

UART Communication

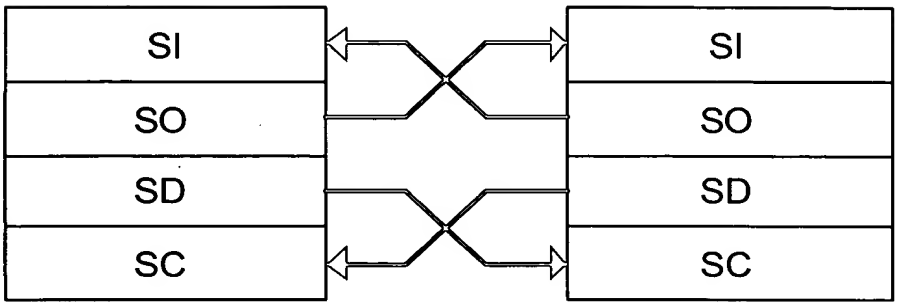


Fig. 107

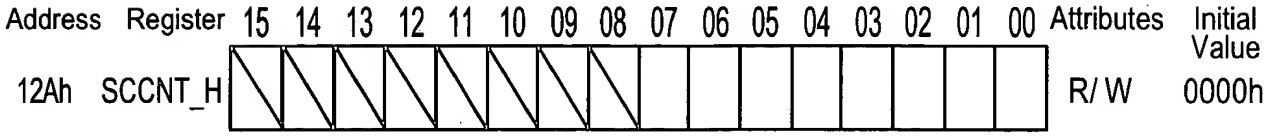


Fig. 108A

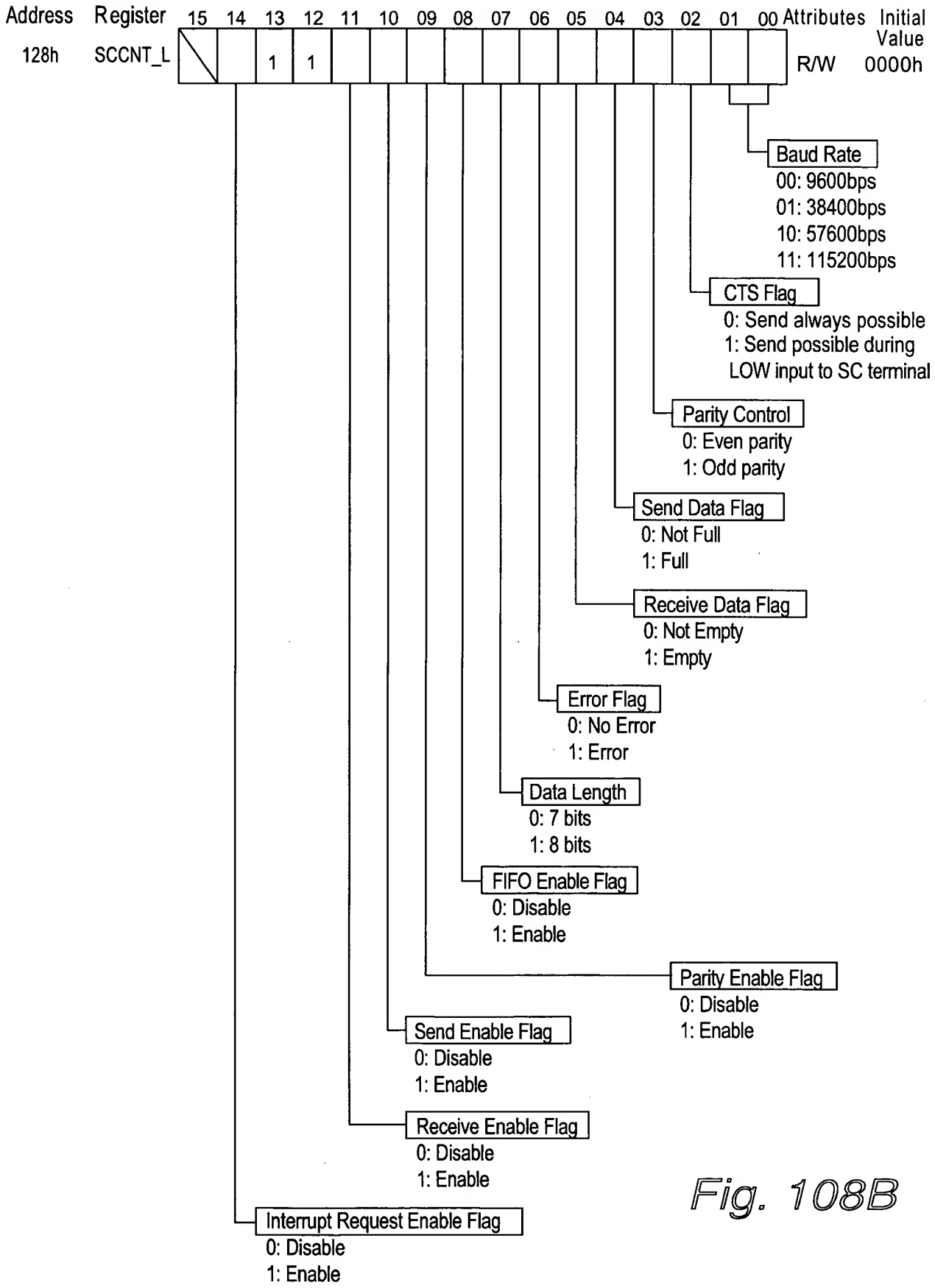

Address
Register
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
Attributes
Initial Value
128h
SCCNT_L
1
1
R/W
0000h
Baud Rate
00: 9600bps
01: 38400bps
10: 57600bps
11: 115200bps
CTS Flag
0: Send always possible
1: Send possible during LOW input to SC terminal
Parity Control
0: Even parity
1: Odd parity
Send Data Flag
0: Not Full
1: Full
Receive Data Flag
0: Not Empty
1: Empty
Error Flag
0: No Error
1: Error
Data Length
0: 7 bits
1: 8 bits
FIFO Enable Flag
0: Disable
1: Enable
Parity Enable Flag
0: Disable
1: Enable
Send Enable Flag
0: Disable
1: Enable
Receive Enable Flag
0: Disable
1: Enable
Interrupt Request Enable Flag
0: Disable
1: Enable

Fig. 108B

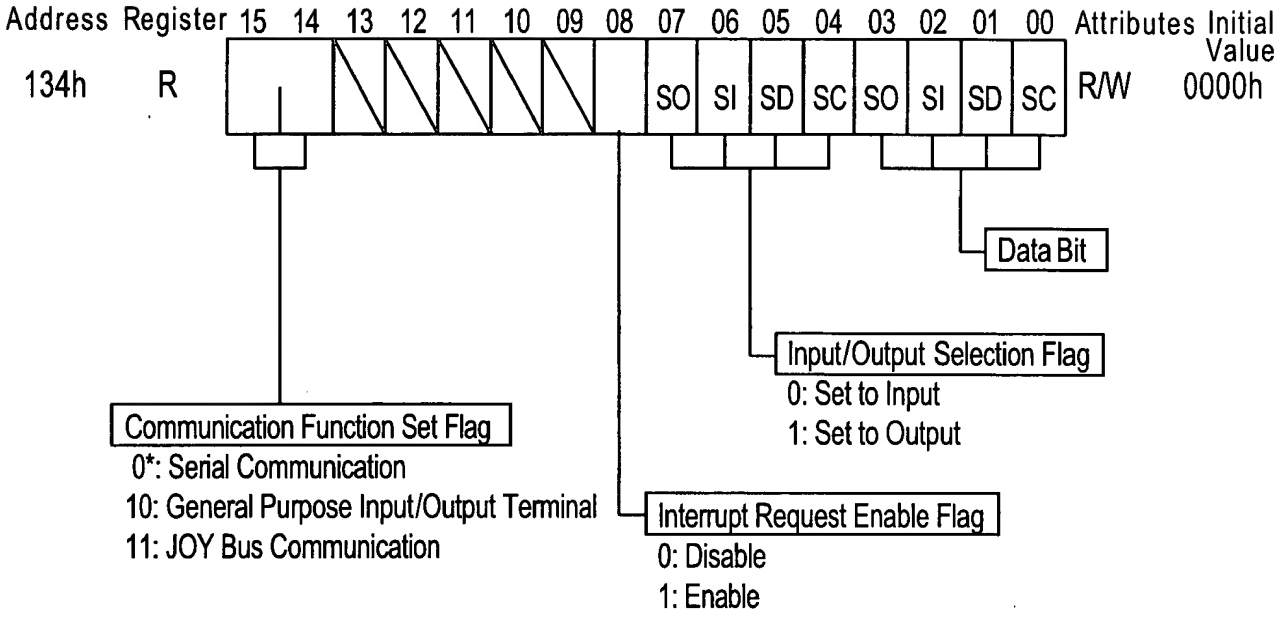


Fig. 109

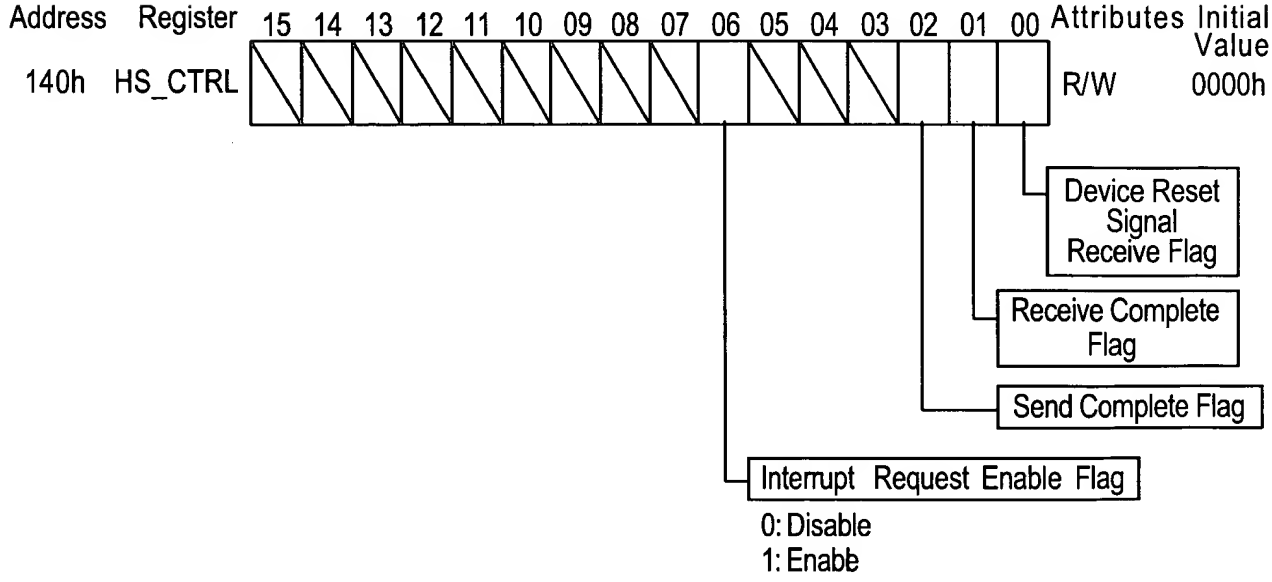


Fig. 110

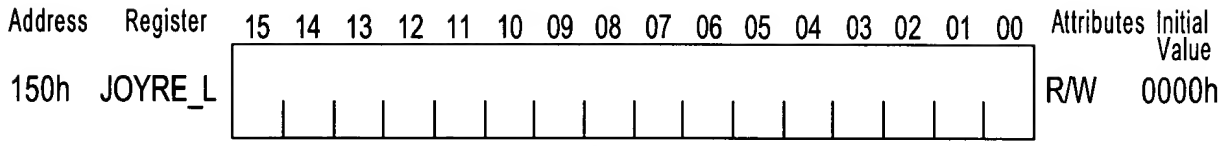


Fig. 111A

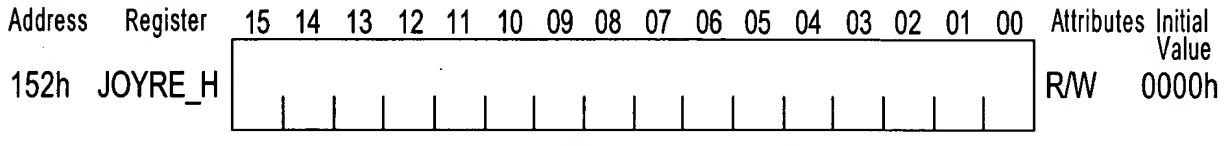


Fig. 111B

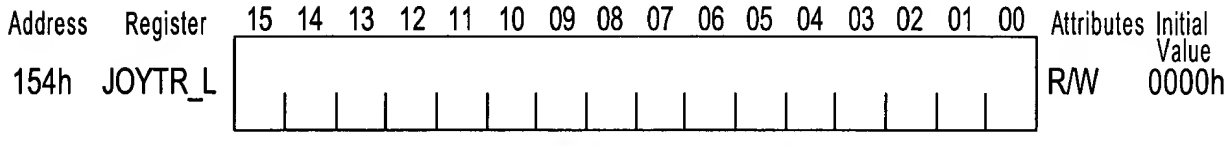


Fig. 112A

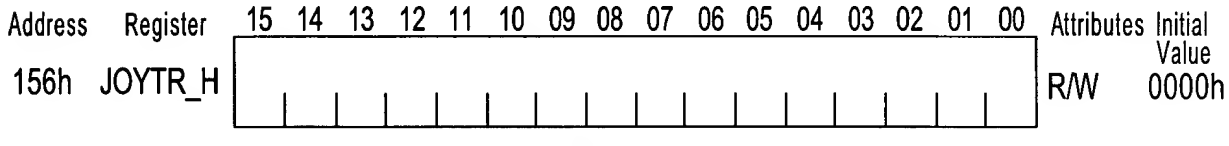


Fig. 112B

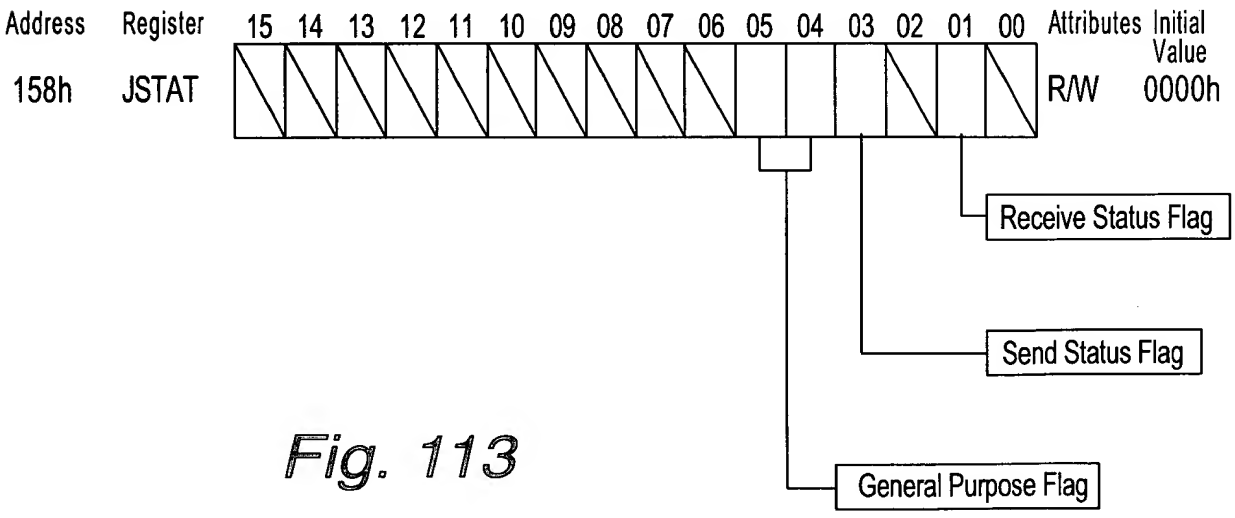


Fig. 113

Device Reset

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	1	1	1	1	1	1	1	1	Command 255(FFh)
Send	1	0	0	0	0	0	0	0	0	Type Number 0400h
	2	0	0	0	0	0	1	0	0	
	3	Lower 8 bits of Register JSTAT								Communication Status

Fig. 114

Type/Status Data Request

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	0	0	0	0	0	Command 0(00h)
Send	1	0	0	0	0	0	0	0	0	Type Number 0400h
	2	0	0	0	0	0	1	0	0	
	3	Lower 8 bits of Register JSTAT								Communication Status

Fig. 115

AGB Data Write

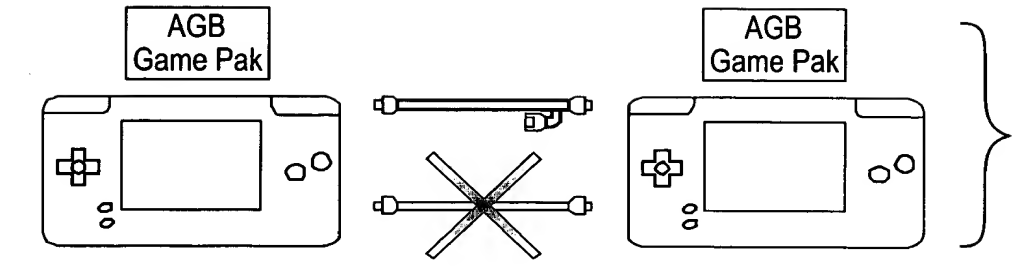
Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	1	0	1	0	1	Command 21(15h)
Receive	2	Lower 8 bits of receive data Register JOYRE_L								Receive Data
	3	Upper 8 bits of receive data Register JOYRE_L								
	4	Lower 8 bits of receive data Register JOYRE_H								
	5	Upper 8 bits of receive data Register JOYRE_H								
Send	6	Lower 8 bits of Register JSTAT								Communication Status

Fig. 116

AGB Data Read

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	1	0	1	0	0	Command 20(14h)
Send	2	Lower 8 bits of send data Register JOYTR_L								Send Data
	3	Upper 8 bits of send data Register JOYTR_L								
	4	Lower 8 bits of send data Register JOYTR_H								
	5	Upper 8 bits of send data Register JOYTR_H								
	6	Lower 8 bits of Register JSTAT								Communication Status

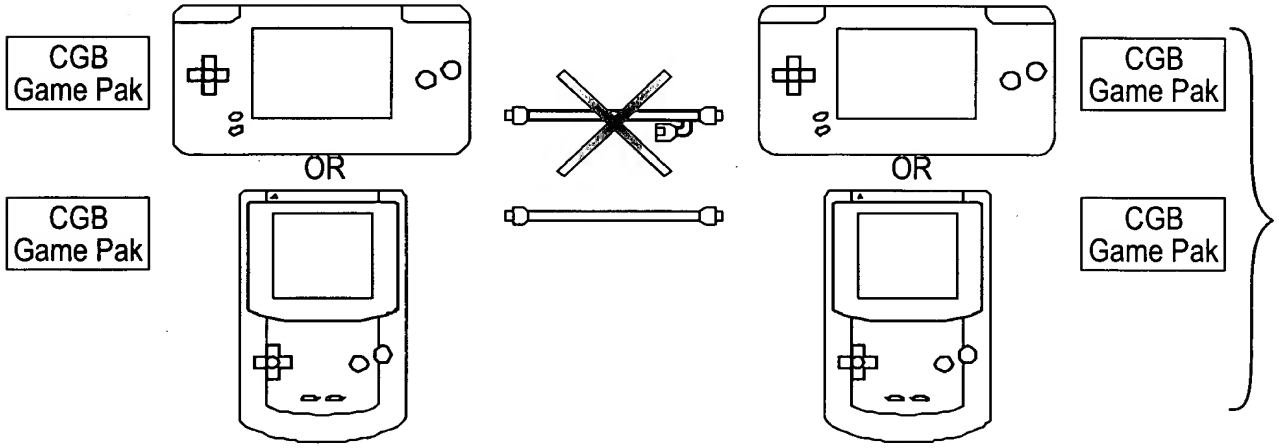
Fig. 117



AGB Cable

MGB/CGB Cable

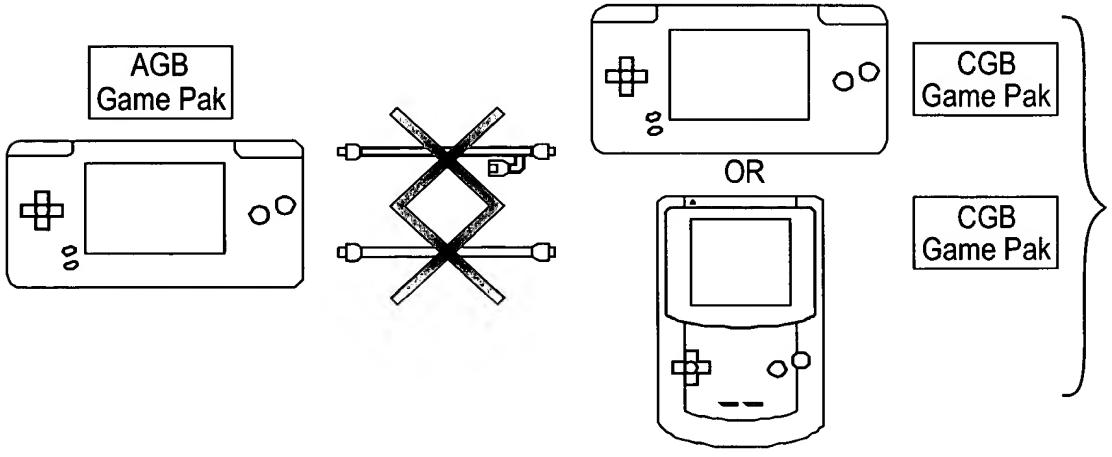
Fig. 118A



AGB Cable

MGB/CGB Cable

Fig. 118B



AGB Cable

MGB/CGB Cable

Fig. 118C

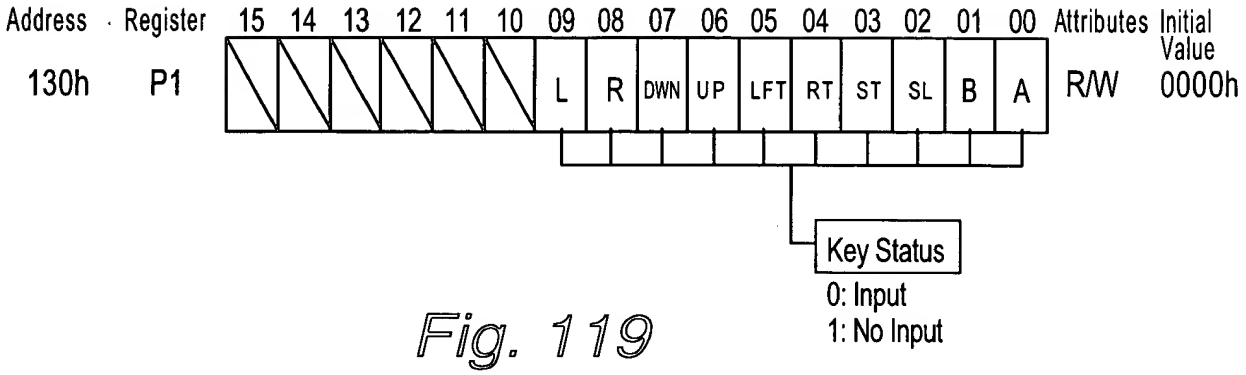


Fig. 119

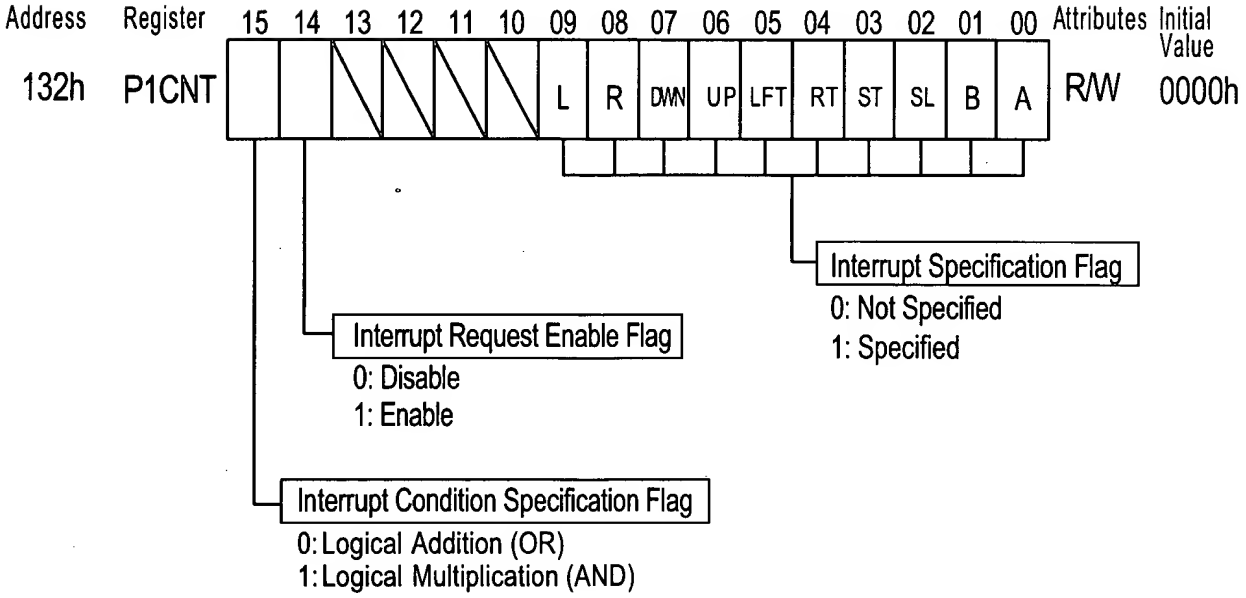


Fig. 120

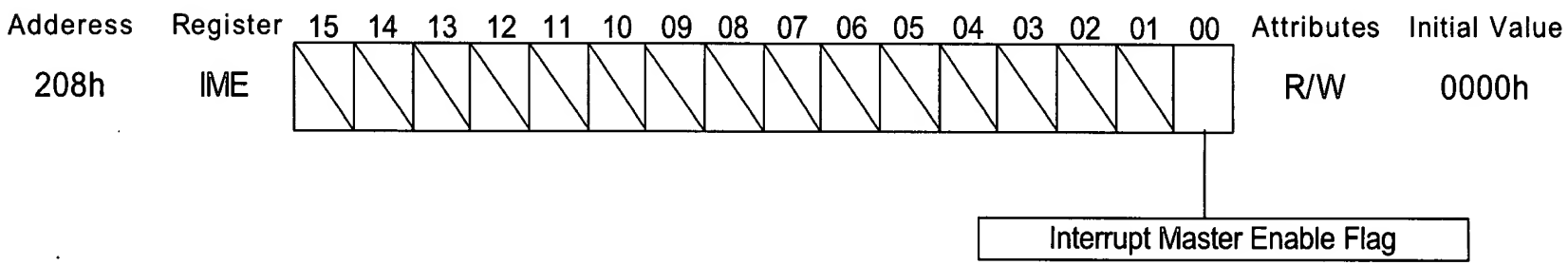


Fig. 121

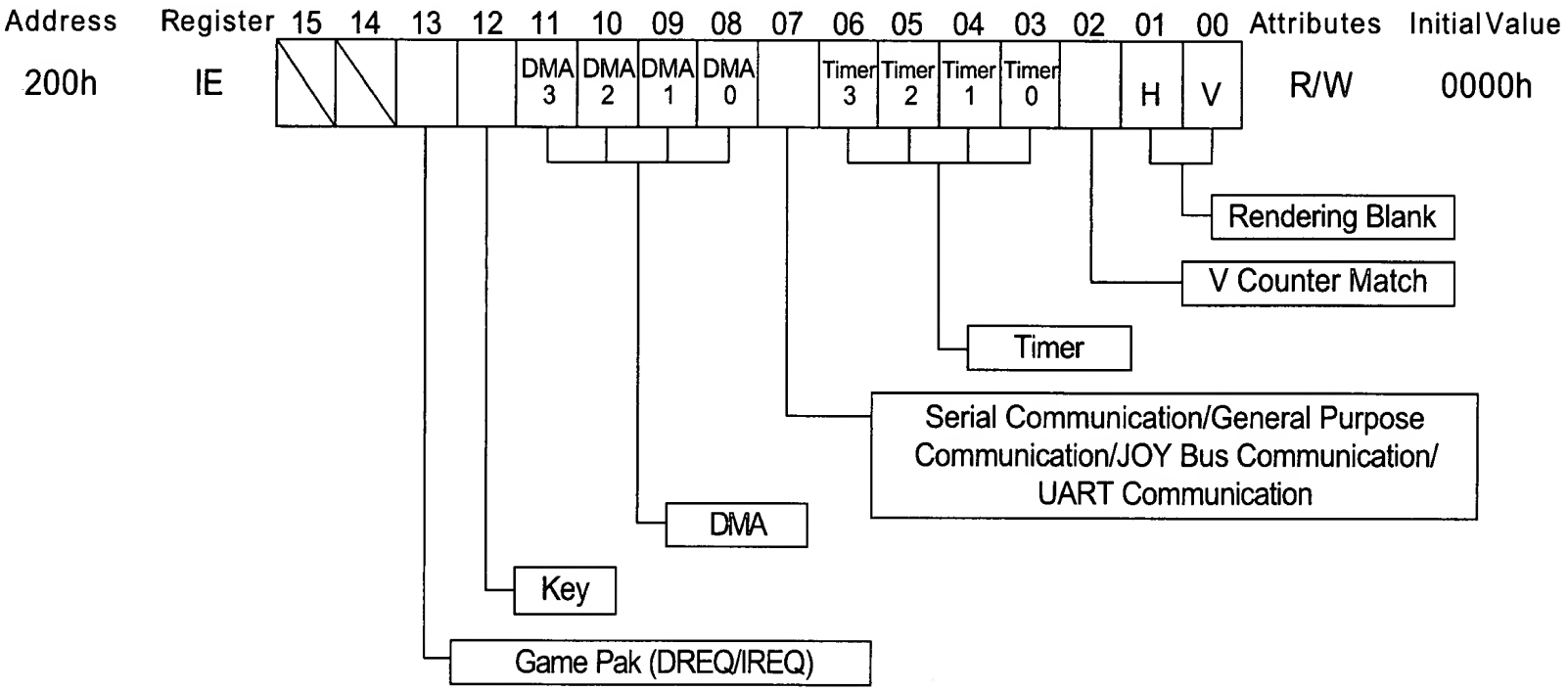


Fig. 122

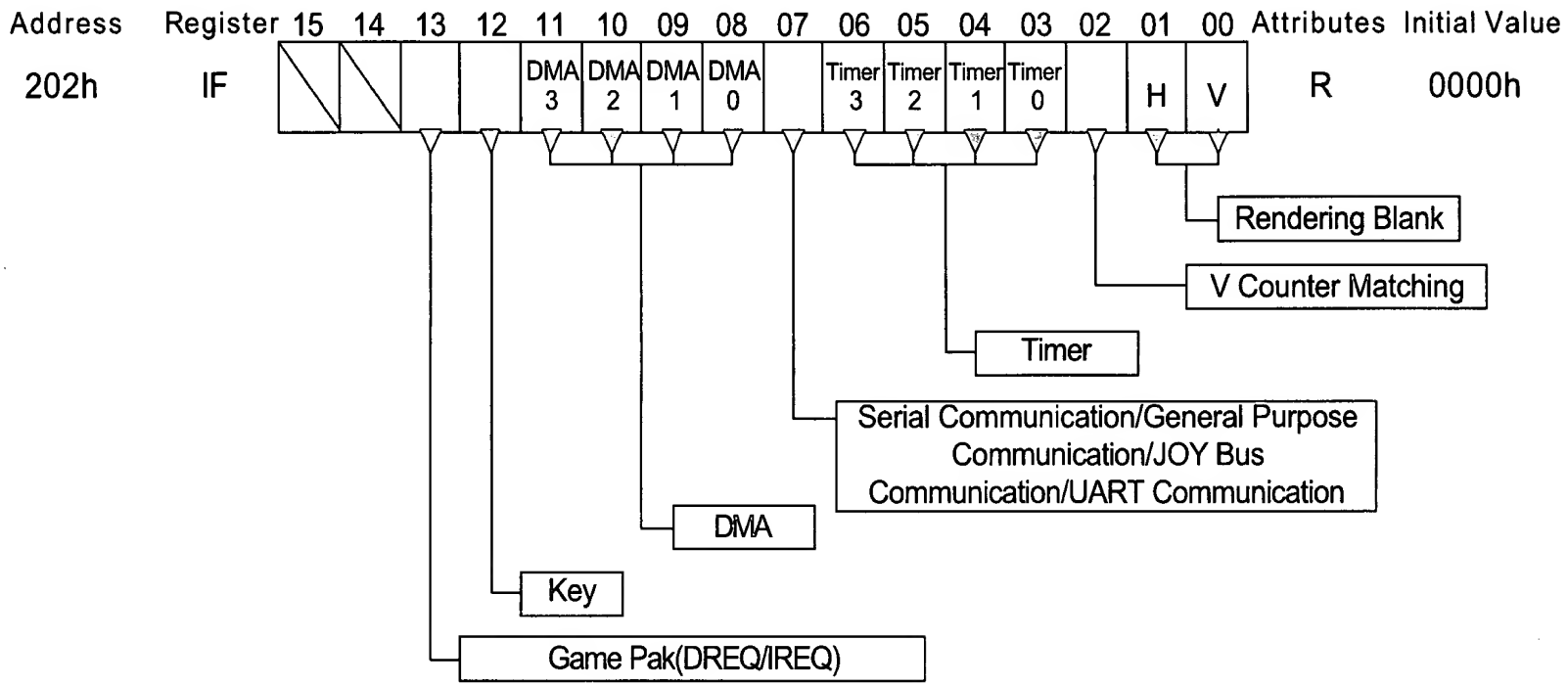


Fig. 123

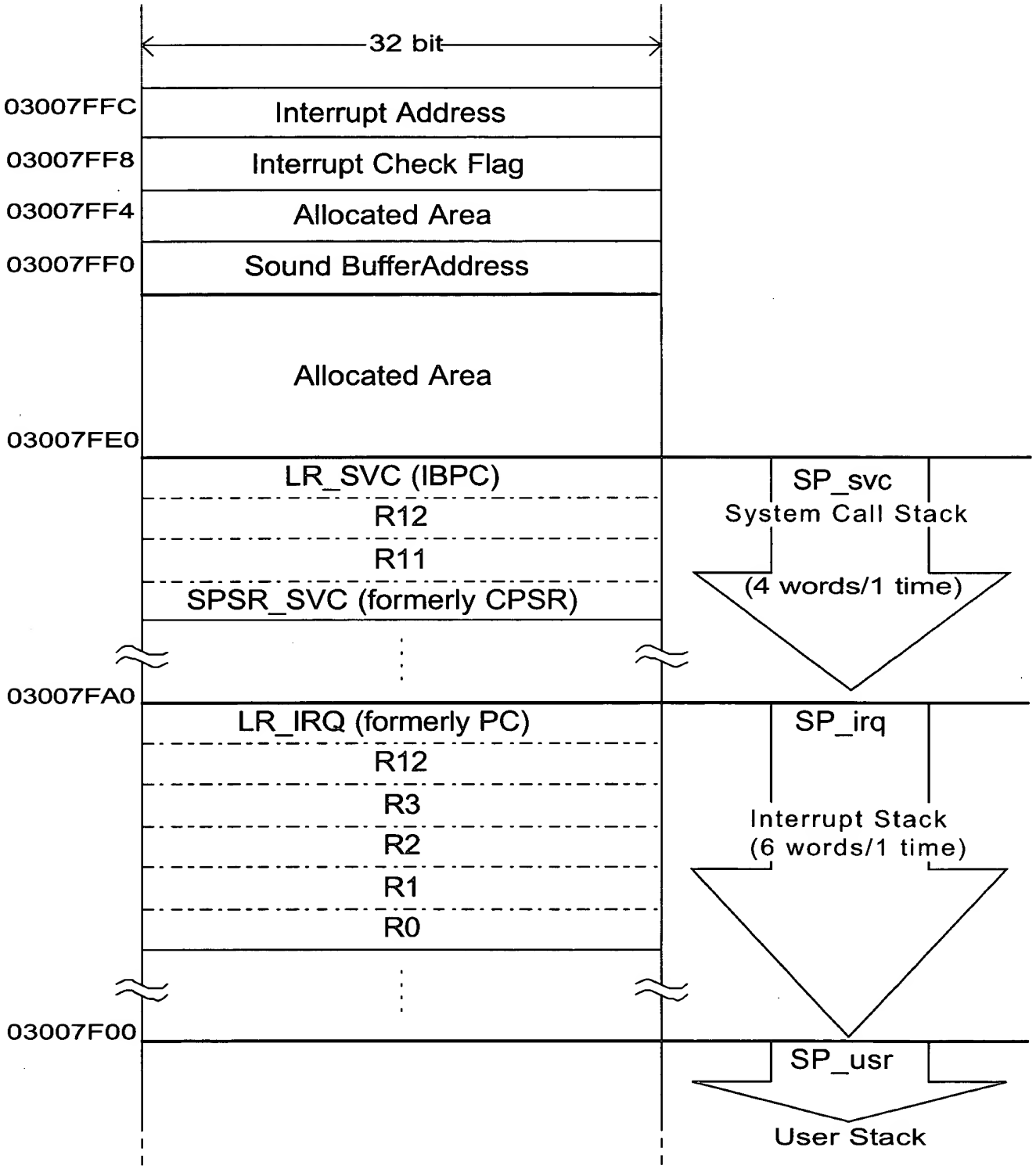

32 bit
03007FFC
Interrupt Address
03007FF8
Interrupt Check Flag
03007FF4
Allocated Area
03007FF0
Sound BufferAddress
Allocated Area
03007FE0
LR_SVC (IBPC)
R12
R11
SPSR_SVC (formerly CPSR)
SP_svc
System Call Stack
(4 words/1 time)
03007FA0
LR_IRQ (formerly PC)
R12
R3
R2
R1
R0
SP_irq
Interrupt Stack
(6 words/1 time)
03007F00
SP_usr
User Stack

Fig. 124

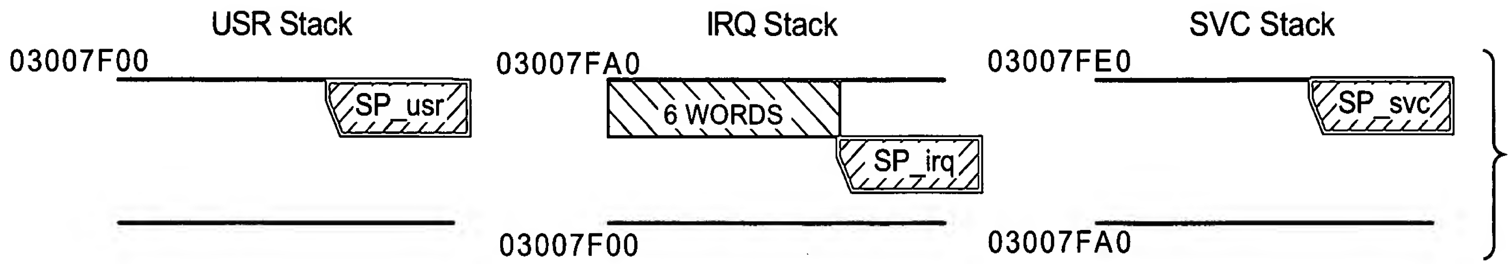


Fig. 125A

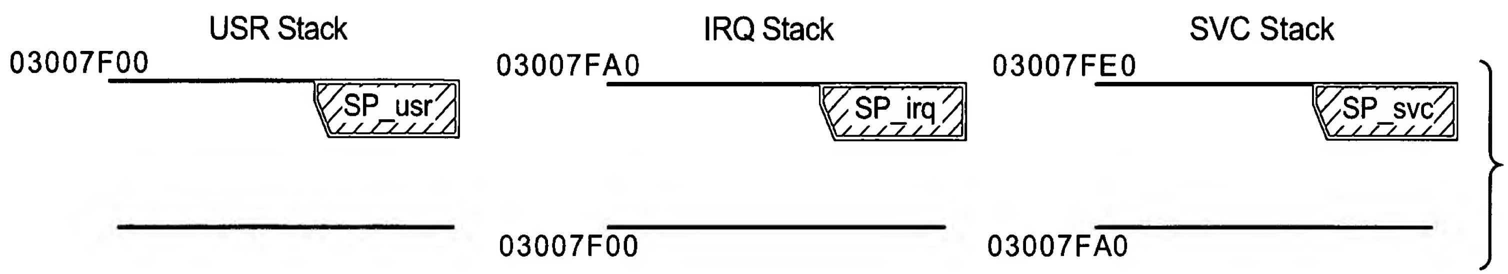


Fig. 125B

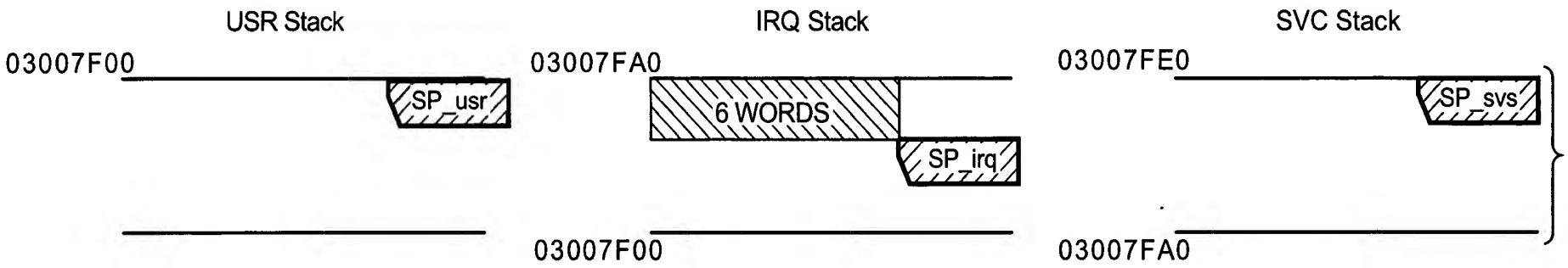


Fig. 126A

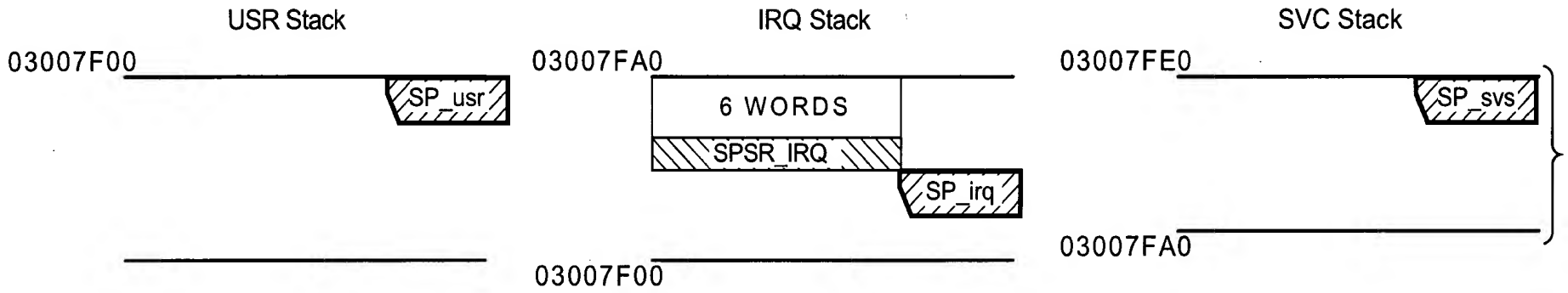


Fig. 126B

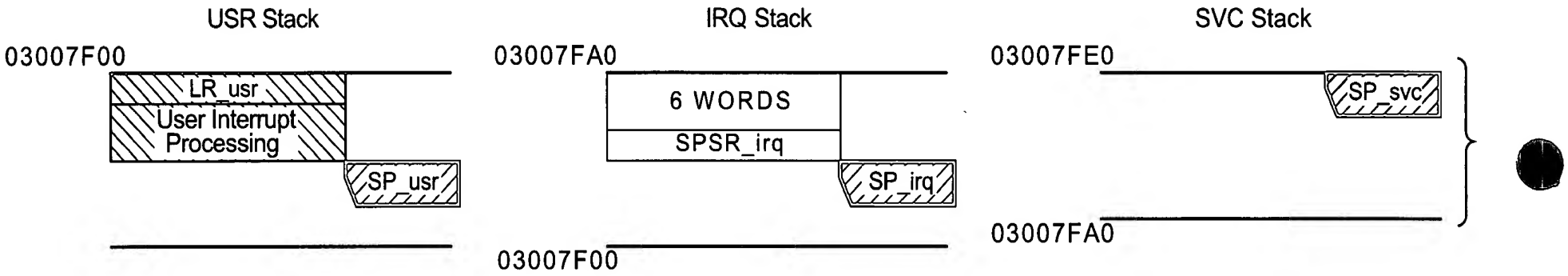


Fig. 126C

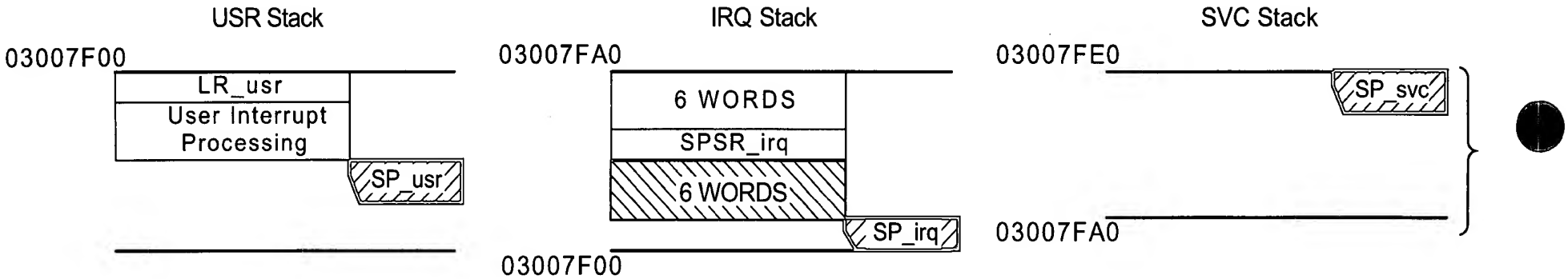


Fig. 126D

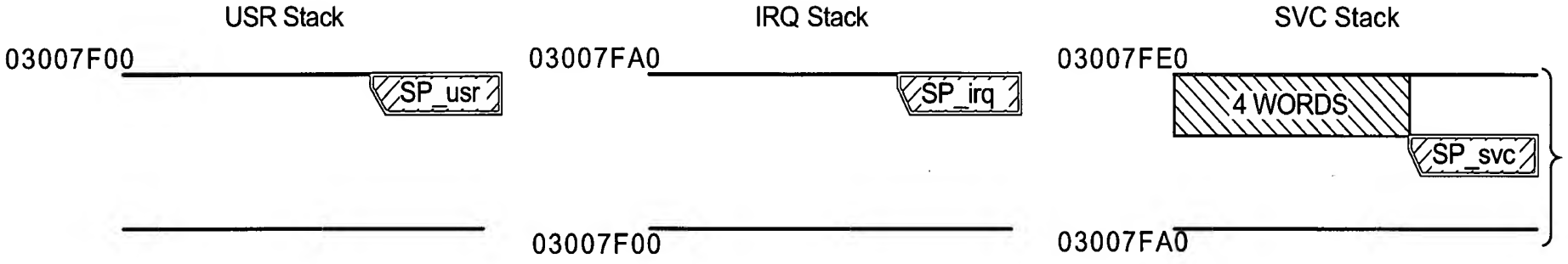


Fig. 127A

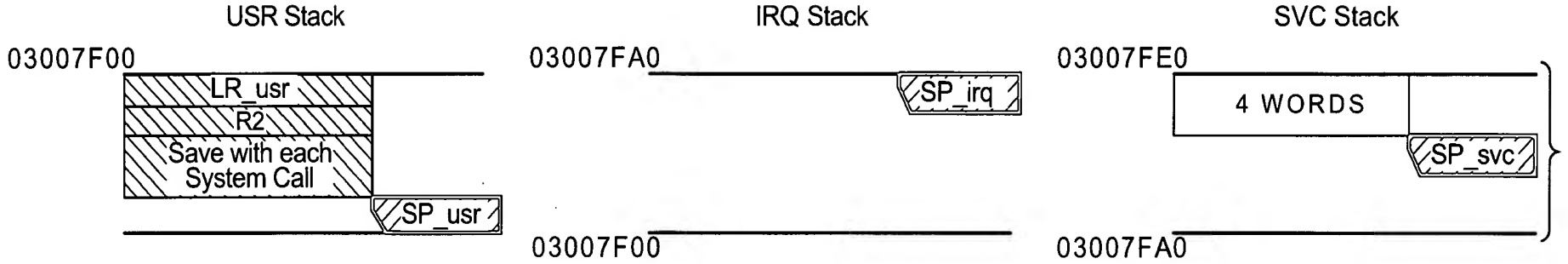


Fig. 127B

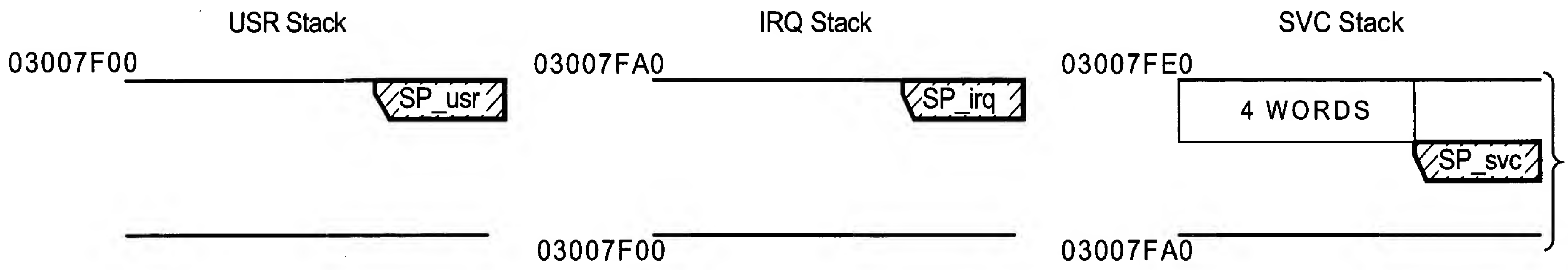


Fig. 127C

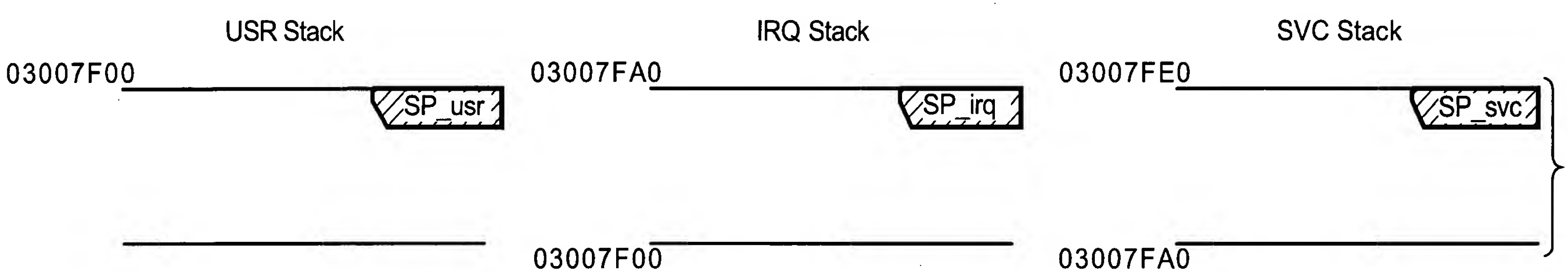


Fig. 127D

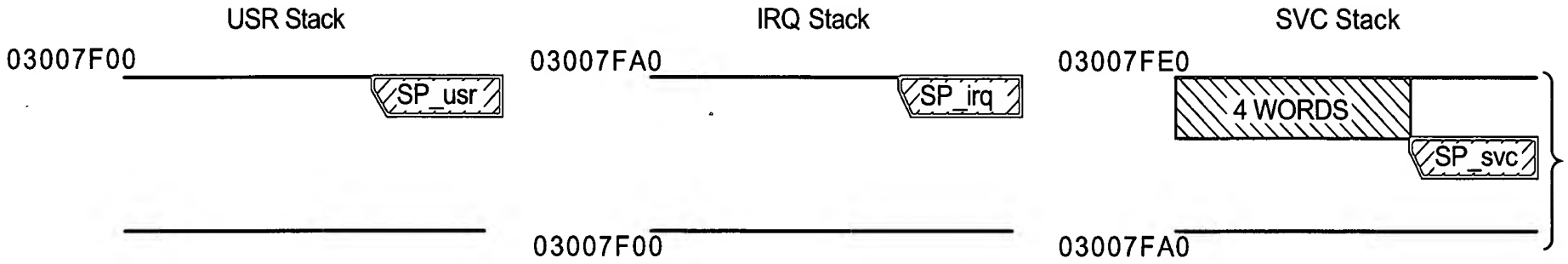


Fig. 128A

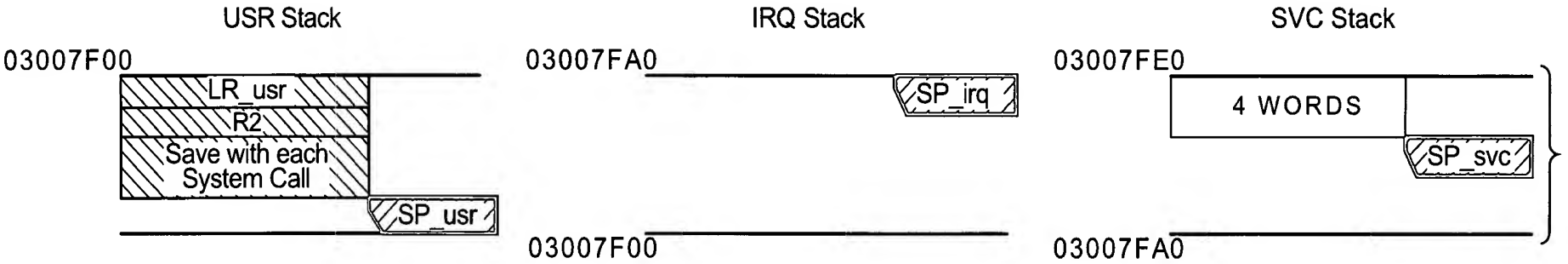


Fig. 128B

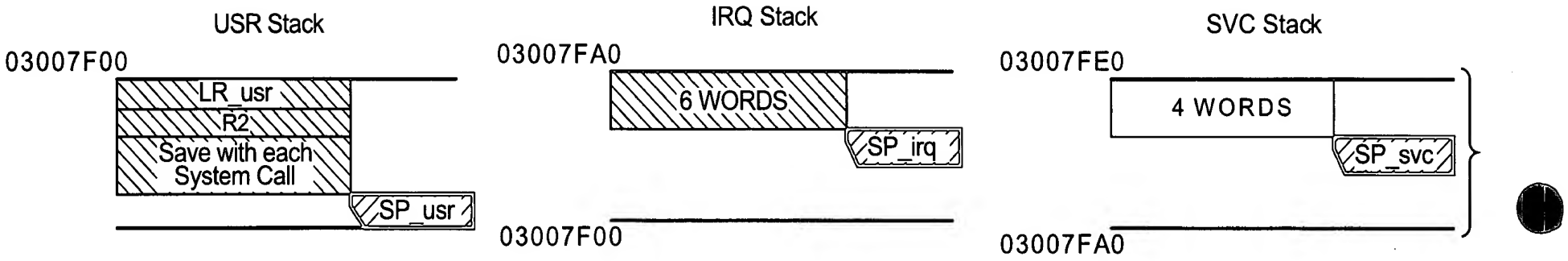


Fig. 128C

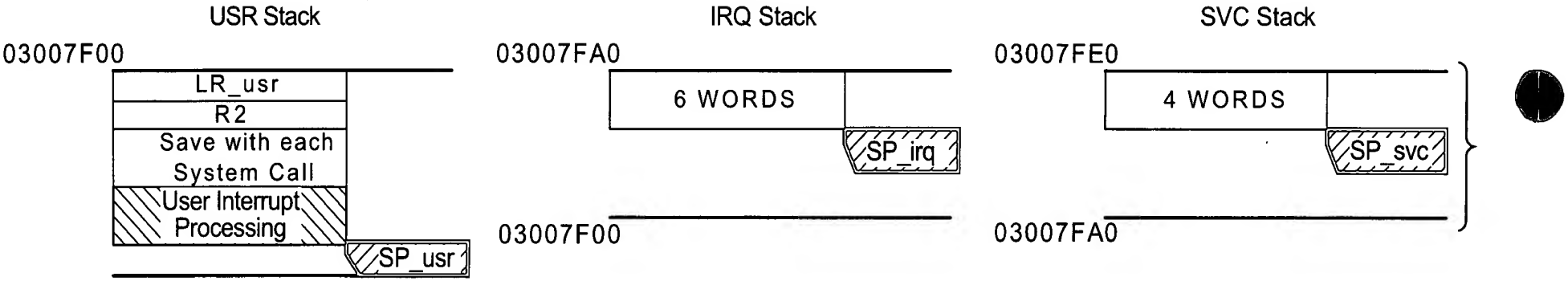


Fig. 128D

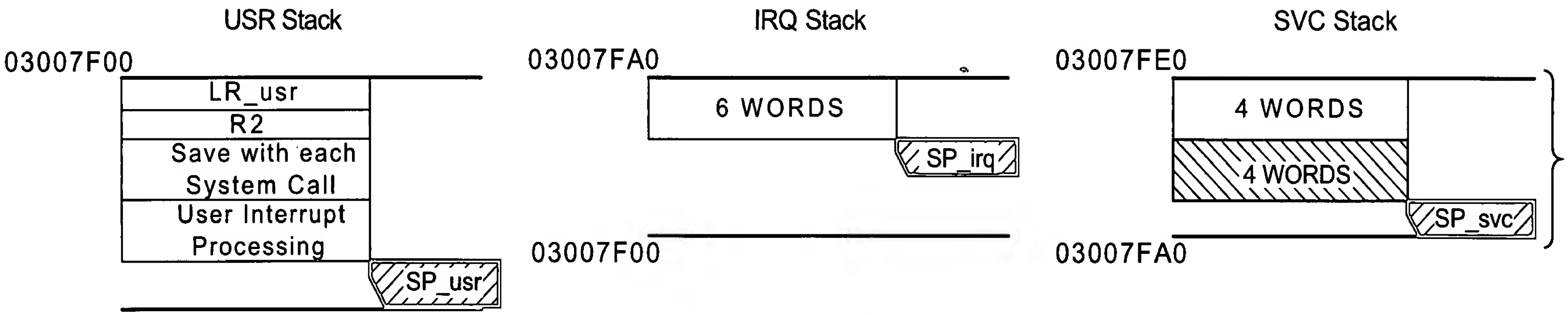


Fig. 128E

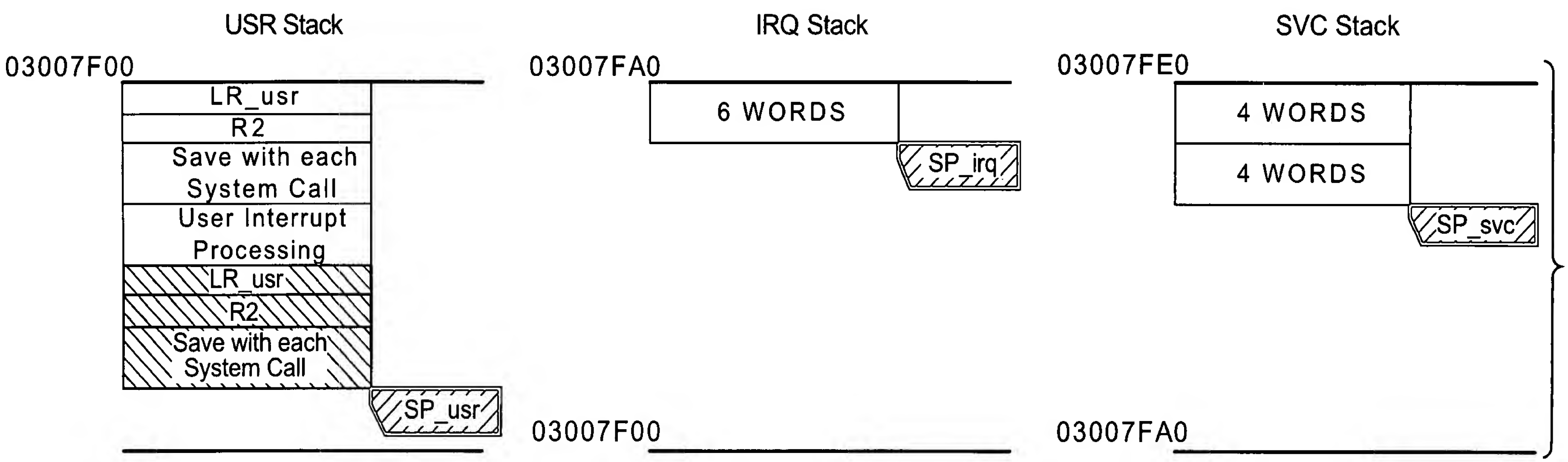


Fig. 128F

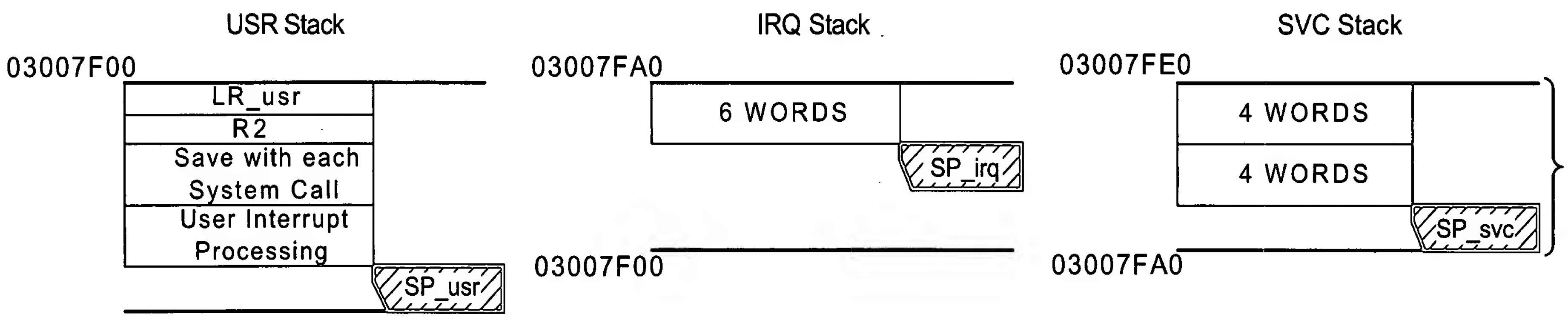


Fig. 128G

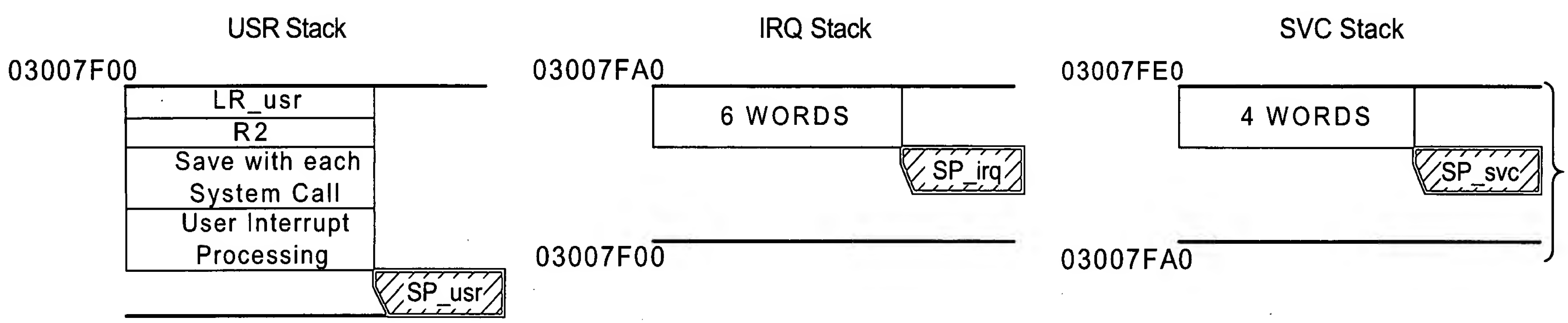


Fig. 128H

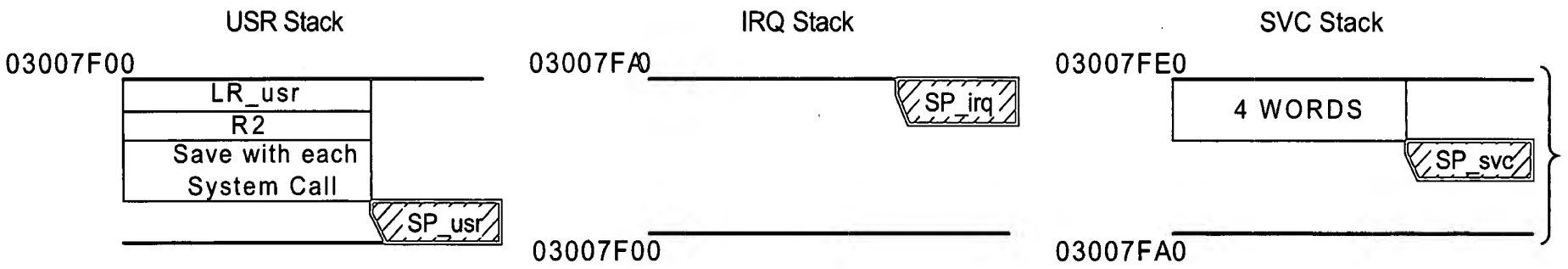


Fig. 128I

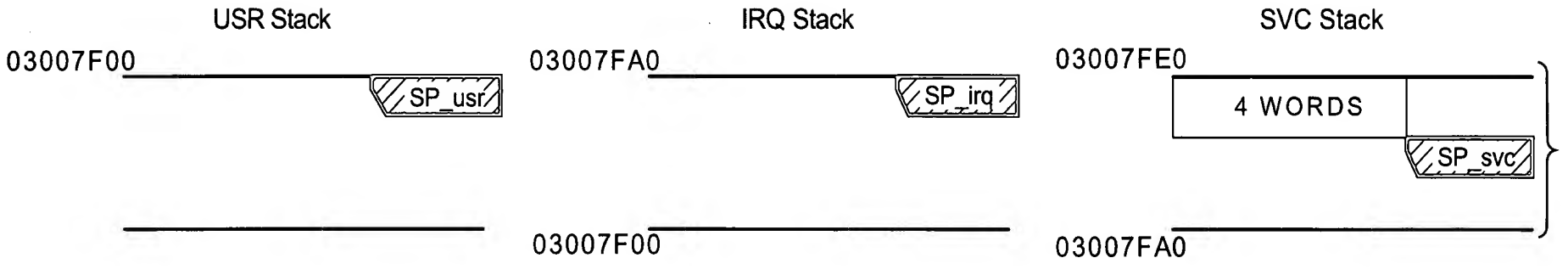


Fig. 128J

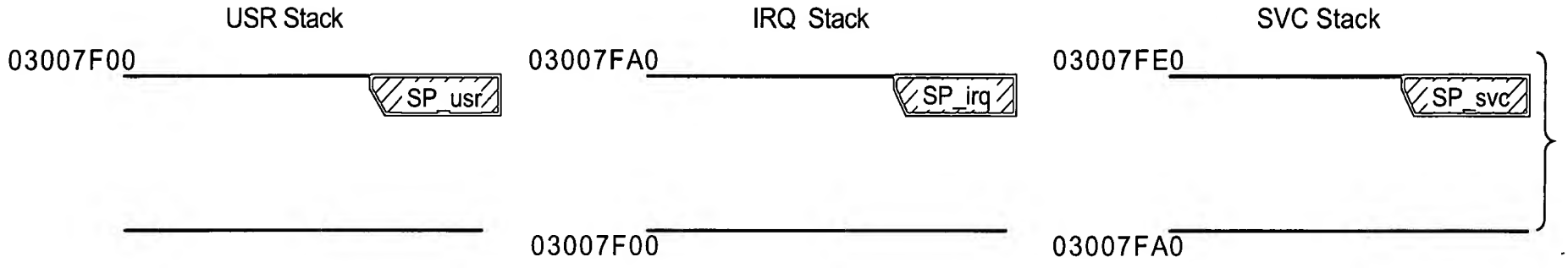


Fig. 128K

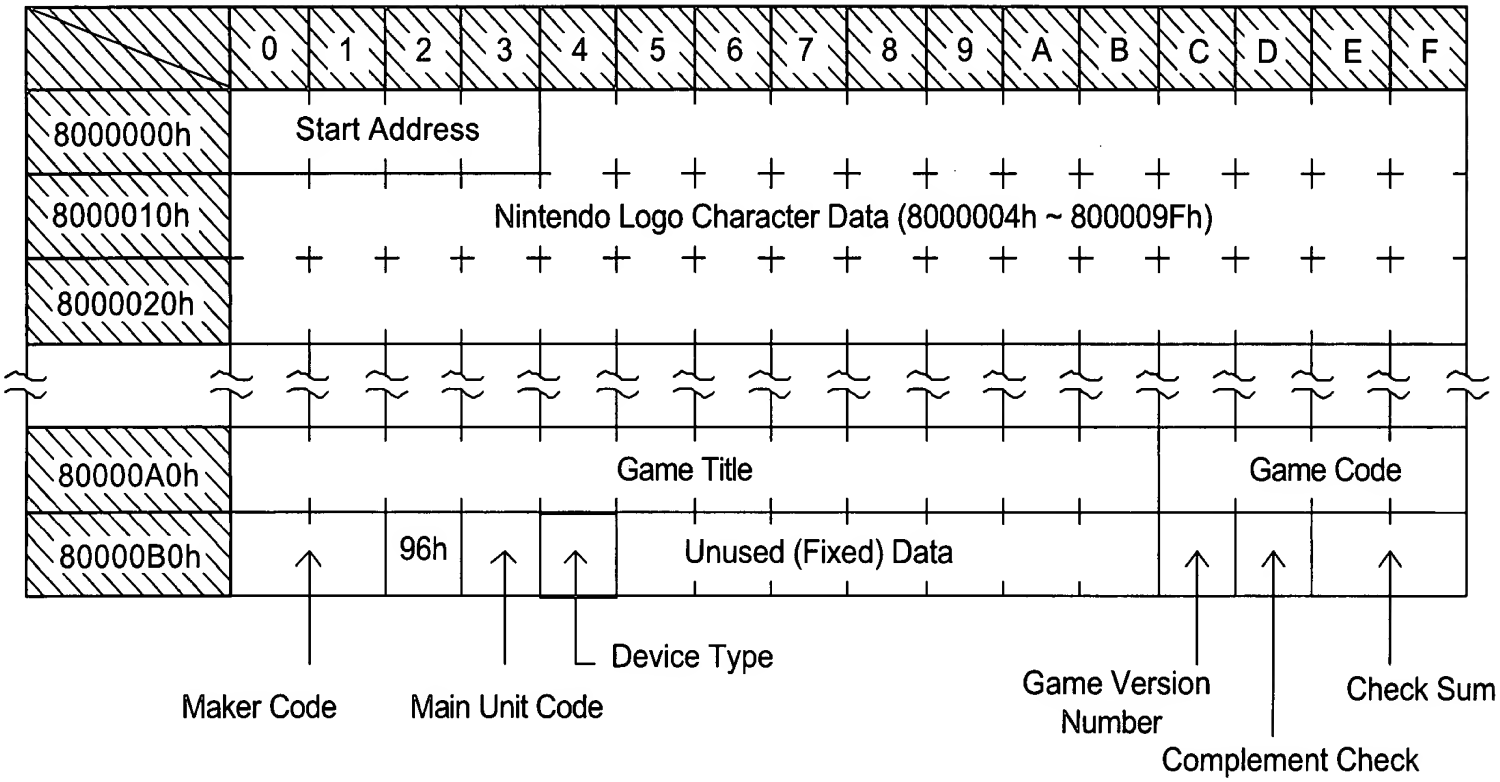
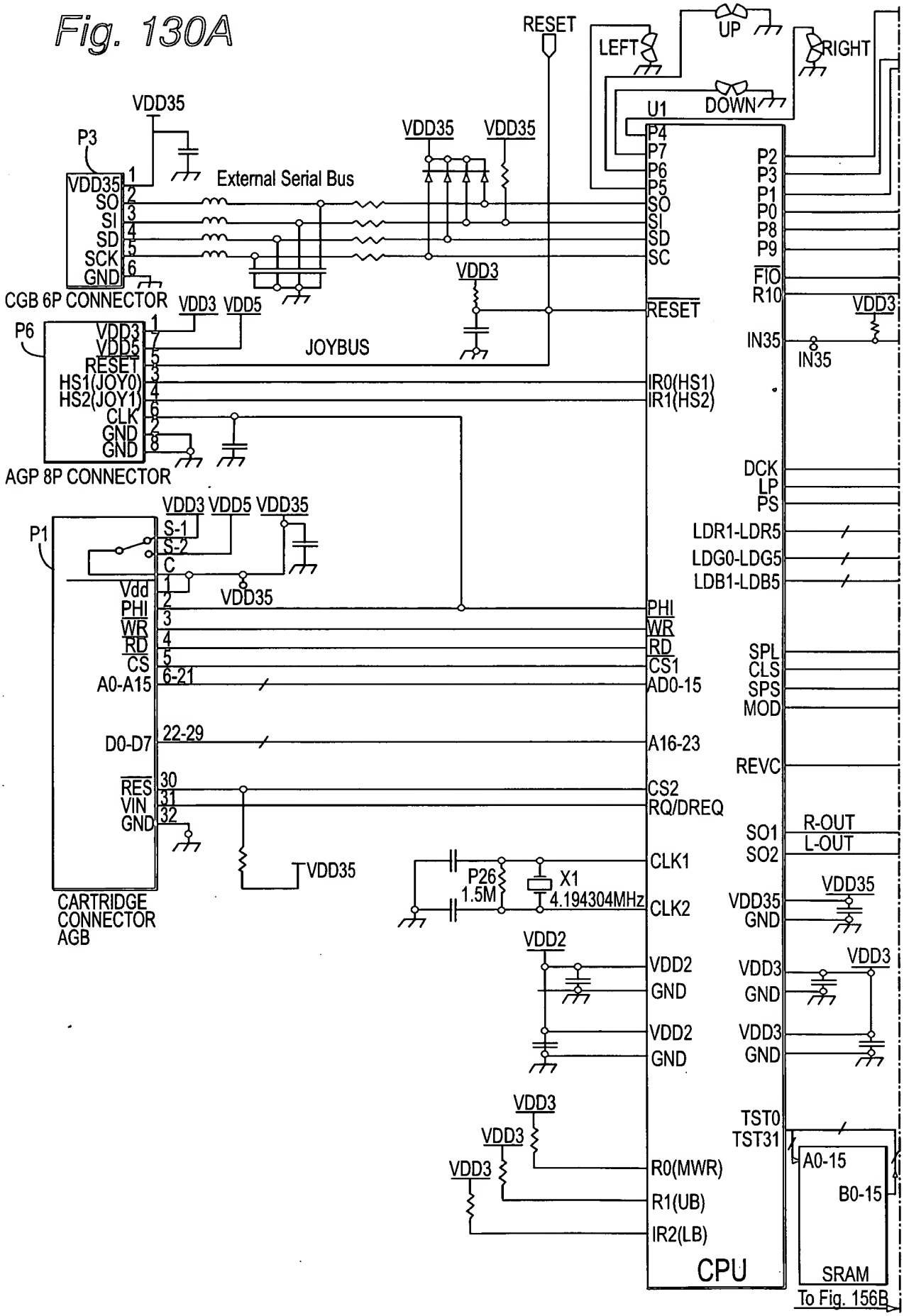


Fig. 129

Fig. 130A


RESET
LEFT
UP
RIGHT
DOWN
U1
VDD35
P3
External Serial Bus
VDD35
VDD35
VDD3
CGB 6P CONNECTOR
VDD3
VDD5
P6
JOYBUS
AGP 8P CONNECTOR
P1
VDD3
VDD5
VDD35
S-1
S-2
C
Vdd
PHI
WR
RD
CS
A0-A15
D0-D7
RES
VIN
GND
6-21
22-29
30
31
32
VDD35
CARTRIDGE CONNECTOR AGB
P26
1.5M
X1
4.194304MHz
VDD2
GND
VDD3
GND
R0(MWR)
R1(UB)
IR2(LB)
CPU
P4
P7
P6
P5
SO
SI
SD
SC
RESET
IR0(HS1)
IR1(HS2)
PHI
WR
RD
CS1
AD0-15
A16-23
CS2
RQ/DREQ
CLK1
CLK2
P2
P3
P1
P0
P8
P9
FIO
R10
IN35
IN35
DCK
LP
PS
LDR1-LDR5
LDG0-LDG5
LDB1-LDB5
SPL
CLS
SPS
MOD
REVC
SO1
SO2
R-OUT
L-OUT
VDD35
GND
VDD3
GND
TST0
TST31
A0-15
B0-15
SRAM
To Fig. 156B

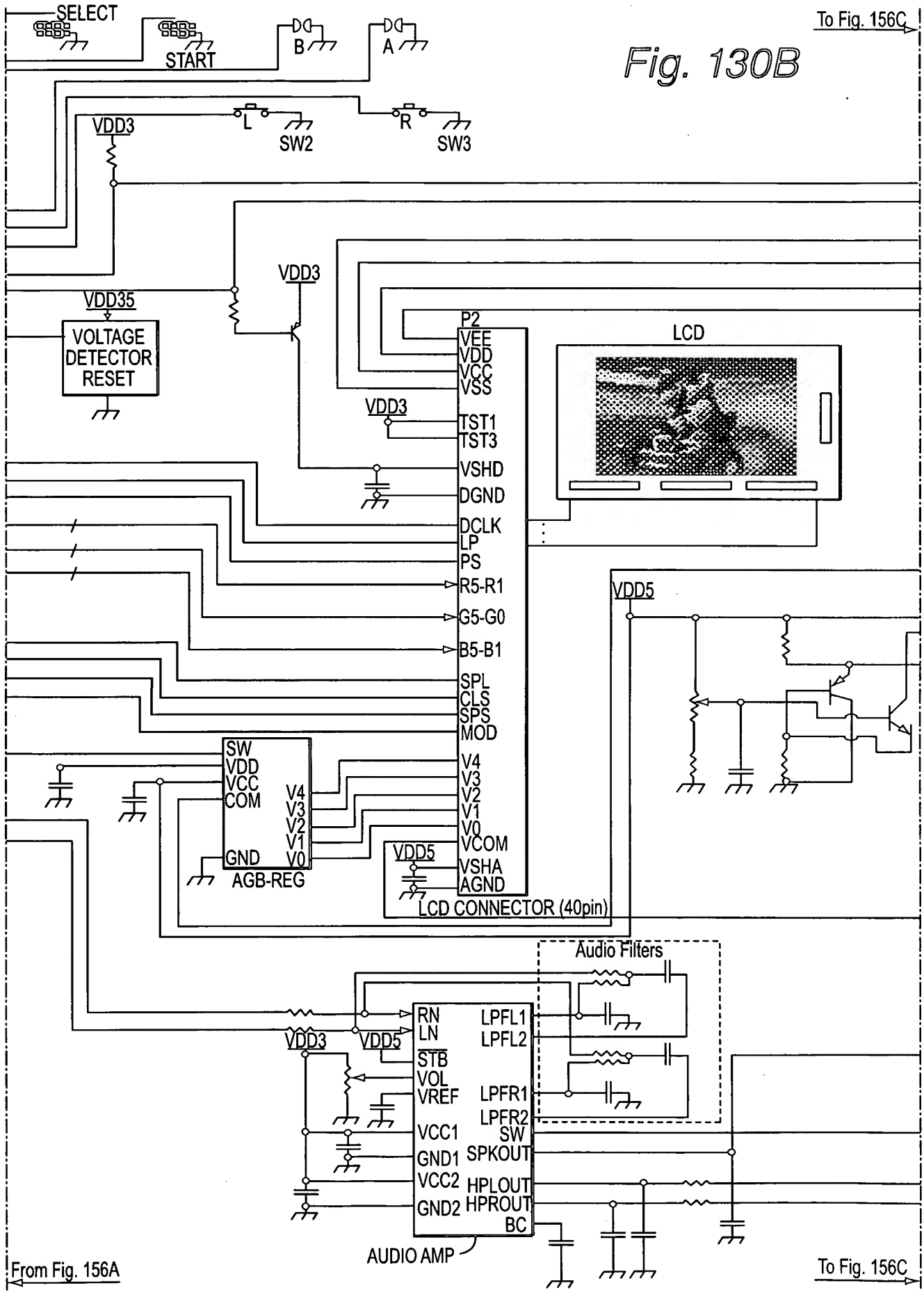

SELECT
START
B
A
To Fig. 156C
VDD3
L
SW2
R
SW3
VDD3
VDD35
VOLTAGE DETECTOR RESET
P2
VEE
VDD
VCC
VSS
LCD
VDD3
TST1
TST3
VSHD
DGND
DCLK
LP
PS
R5-R1
G5-G0
B5-B1
SPL
CLS
SPS
MOD
VDD5
SW
VDD
VCC
COM
GND
V4
V3
V2
V1
V0
AGB-REG
V4
V3
V2
V1
V0
VCOM
VDD5
VSHA
AGND
LCD CONNECTOR (40pin)
Audio Filters
RN
LN
STB
VOL
VREF
VCC1
GND1
VCC2
GND2
VDD3
VDD5
LPFL1
LPFL2
LPFR1
LPFR2
SW
SPKOUT
HPLOUT
HPROUT
BC
AUDIO AMP
From Fig. 156A
To Fig. 156C

Fig. 130B

Fig. 130C

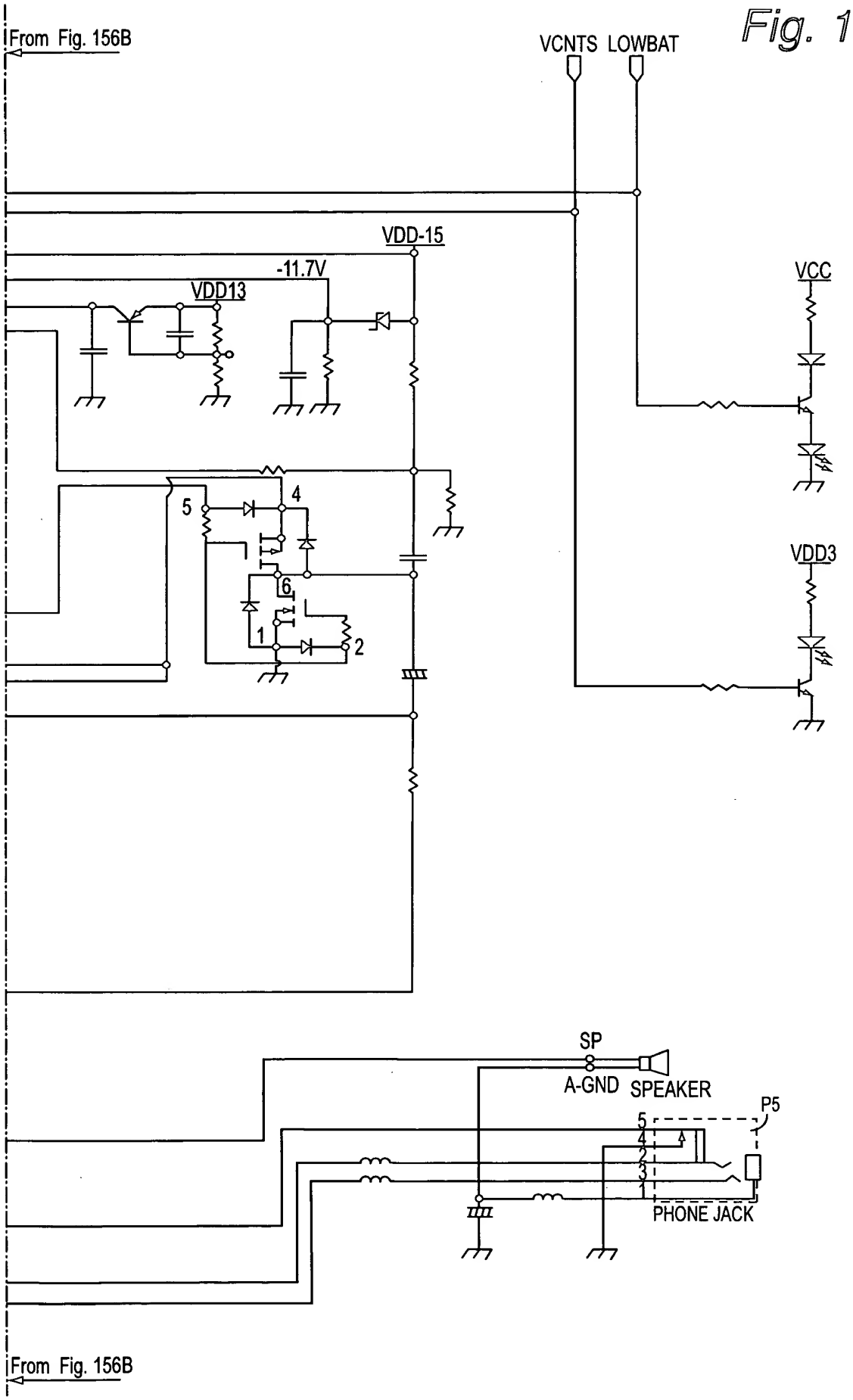

From Fig. 156B
VCNTS
LOWBAT
VDD-15
-11.7V
VDD13
VCC
VDD3
5
4
6
1
2
SP
A-GND
SPEAKER
P5
5
4
2
3
1
PHONE JACK
From Fig. 156B

Fig. 131A

Addr		D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Figure in App.
00	DISPCNT	Window Display Flag			Display Flag					Forced Blank	OBJ Map Format	OB J Hoff	Frame Buffer No .	CGB mode	BG Mode			R/W	0080h	Fig. 29
		OBJ	W IN1	WIN0	OBJ	BG3	BG2	BG1	BG0											
04	DISPSTAT	V Count Setting								-	-	V counter Match Interrupt	HBlank Interrupt	VBlank Interrupt	V Counter Eval.	HBlank Status	VBlank Status	R/W	0000h	Fig. 28
06	VCOUNT	-	-	-	-	-	-	-	-	V Counter Value								R	0000h	Fig. 27
08	BG0CNT	Size		-	Screen Base Block					Color Mode	Mosaic	0	0	Character Base Block		Priority		R/W	0000h	Fig. 32A
0A	BG1CNT	Size		-	Screen Base Block					Color Mode	Mosaic	0	0	Character Base Block		Priority		R/W	0000h	Fig. 32A
0C	BG2CNT	Size		Area Overflow	Screen Base Block					Color Mode	Mosaic	0	0	Character Base Block		Priority		R/W	0000h	Fig. 32B
0E	BG3CNT	Size		Area Overflow	Screen Base Block					Color Mode	Mosaic	0	0	Character Base Block		Priority		R/W	0000h	Fig. 32B
10	BG0HOFS	-	-	-	-	-	-	-	Horizontal Offset									W	0000h	Fig. 45A
12	BG0VOFS	-	-	-	-	-	-	-	Vertical Offset									W	0000h	Fig. 45B
14	BG1HOFS	-	-	-	-	-	-	-	Horizontal Offset									W	0000h	Fig. 45A
16	BG1VOFS	-	-	-	-	-	-	-	Vertical Offset									W	0000h	Fig. 45B
18	BG2HOFS	-	-	-	-	-	-	-	Horizontal Offset									W	0000h	Fig. 45A
1A	BG2VOFS	-	-	-	-	-	-	-	Vertical Offset									W	0000h	Fig. 45B
1C	BG3HOFS	-	-	-	-	-	-	-	Horizontal Offset									W	0000h	Fig. 45A
1E	BG3VOFS	-	-	-	-	-	-	-	Vertical Offset									W	0000h	Fig. 45B
20	BG2PA	dx: Distance moved Along same line in x direction																W	0100h	Fig. 44A
22	BG2PB	dmx: Distance moved Along next line in x direction																W	0000h	Fig. 44B
24	BG2PC	dy: Distance moved Along same line in y direction																W	0100h	Fig. 44C
26	BG2PD	dmy: Distance moved Along next line in y direction																W	0000h	Fig. 44D

Fig. 131B

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Fig. in App
28	BG2X _L	x-Coordinate of reference Starting point (rotation/scaling results)																	0000h	Fig. 43A
2A	BG2X _H	-	-	-	-	x-Coordinate of reference Starting point (rotation/scaling results)												W	0000h	Fig. 43B
2C	BG2Y_L	y-Coordinate of reference Starting point (rotation/scaling results)																	0000h	Fig. 43C
2E	BG2Y_H	-	-	-	-	y-Coordinate of reference Starting point (rotation/scaling results)												W	0000h	Fig. 43D
30	BG3PA	dx: Distance moved Along same line in x direction																W	0100h	Fig. 44A
32	BG3PB	dmx: Distance moved Along next line in x direction																W	0000h	Fig. 44B
34	BG3PC	dy: Distance moved Along same line in y direction																	0000h	Fig. 44C
36	BG3PD	dmy: Distance moved Along next line in y direction																W	0100h	Fig. 44D
38	BG3X_L	x-Coordinate of reference Starting point (rotation/scaling results)																	0000h	Fig. 43A
3A	BG3X_H	-	-	-	-	x-Coordinate of reference Starting point (rotation/scaling results)												W	0000h	Fig. 43B
3C	BG3Y_L	y-Coordinate of reference Starting point (rotation/scaling results)																	0000h	Fig. 43C
3E	BG3Y_H	-	-	-	-	y-Coordinate of reference Starting point (rotation/scaling results)												W	0000h	Fig. 43D
40	WIN0H	Window 0 upper-left x-Coordinate								Window 0 lower-right x-Coordinate								W	0000h	
42	WIN1 H	Window 1 upper-left x-Coordinate								Window 1 lower-right x-Coordinate								W	0000h	
44	WIN0 V	Window 0 upper-left y-Coordinate								Window 0 lower-right y-Coordinate								W	0000h	
46	WIN1 V	Window 1 upper-left y-Coordinate								Window 1 lower-right y-Coordinate								W	0000h	
				Control for Inside of Window 1																
48	WININ	-	-	Special Effects	OBJ	BG3	BG2	BG1	BG0	-	-	Special Effects	OBJ	BG3	BG2	BG1	BG 0	R/W	0000h	Fig. 65*
				OBJ Window Control																
4A	WNOUT	-	-	Special Effects	OBJ	BG3	BG2	BG1	BG0	-	-	Special Effects	OB J	BG 3	BG 2	BG 1	BG 0	R/W	0000h	Fig. 66

Fig. 131C

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Fig. in App
4C	MOSAIC	OBJ Mosaic Vertical Size				OBJ Mosaic Horizontal Size				BG Mosaic Vertical Size				BG Mosaic Horizontal Size				W	0000h	Fig. 35
50	BLDMOD	-	-	2nd target pixel BD	2nd target pixel OBJ	2nd target pixel BG3	2nd target pixel BG2	2nd target pixel BG1	2nd target pixel BG0	Type of Color Special Effect		1st target pixel BD	1st target pixel OBJ	1st target pixel BG3	1st target pixel BG2	1st target pixel BG1	1st target pixel BG0	R/W	0000h	Fig. 67
52	COLEV	-	-	-	Color Special Effect Coefficient EVB					-	-	-	Color Special Effect Coefficient EVA						0000h	Fig. 68A
54	COLEY	-	-	-	-	-	-	-	-	-	-	-	Color Special Effect Coefficient EVY					W	0000h	Fig. 68B
60	SG10_L	-	-	-	-	-	-	-	-	NR10								W/R	0000h	Fig. 72A
62	SG10_H	NR12								NR11								W/R	0000h	Fig. 72B
64	SG11	NR14								NR13								W/R	0000h	Fig. 72C
68	SG20	NR22								NR21								W/R	0000h	Fig. 74A
6C	SG21	NR24								NR23								W/R	0000h	Fig. 74B
70	SG30_L	-	-	-	-	-	-	-	-	NR30								W/R	0000h	Fig. 75A
72	SG30_H	NR32								NR31								W/R	0000h	Fig. 75B
74	SG31	NR34								NR33								W/R	0000h	Fig. 75C
78	SG40	NR42								NR41								W/R	0000h	Fig. 77A*
7C	SG41	NR44								NR43								W/R	0000h	Fig. 77B
80	SGCNT0_L	NR51								NR50								W/R		Fig. 78A
82	SGCNT0_H	Direct Sound B FIFO B reset	Direct Sound B TIMER	Direct Sound B L Output	Direct Sound B R Output	Direct Sound A FIFO A reset	Direct Sound A TIMER	Direct Sound A L Output	Direct Sound A R Output	-	-	-	-	DSB Output Ratio	DSA Output Ratio	Sound 1-4 Mix Ratio		W/R	0000h	Fig. 78C
84	SGCNT1	-	-	-	-	-	-	-	-	NR52								W/R	0000h	Fig. 78B
88	SGBIAS	Amplitude Resolution/ Sampling Cycle		-	-	-	-	Bias Level										W/R	0000h	Fig. 79

Fig. 131D

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Fig. in App.
90	SGWR0_L	Step 2				Step 3				Step 0				Step 1				W/R	-	Fig. 76A
92	SGWR0_H	Step 6				Step 7				Step 4				Step 5				W/R	-	Fig. 76B
94	SGWR1_L	Step 10				Step 11				Step 8				Step 9				W/R	-	Fig. 76C
96	SGWR1_H	Step 14				Step 15				Step 12				Step 13				W/R	-	Fig. 76D
98	SGWR2_L	Step 18				Step 19				Step 16				Step 17				W/R		Fig.76E
9A	SGWR2_H	Step 22				Step 23				Step 20				Step 21				W/R	-	Fig. 76F
9C	SGWR3_L	Step 26				Step 27				Step 24				Step 25				W/R	-	Fig.76G
9E	SGWR3_H	Step 30				Step 31				Step 28				Step 29				W/R	-	Fig. 76H
A0	SGFIFOA_L	Sound Data 1								Sound Data0								W	-	Fig. 71A
A2	SGFIFOA_H	Sound Data 3								Sound Data2								W	-	Fig. 72A
A4	SGFIFOB_L	Sound Data 1								Sound Data 0								W	-	Fig. 71A
A6	SGFIFOB_H	Sound Data 3								Sound Data 2								W	-	Fig. 72A
B0	DM0SAD_L																	W	0000h	Fig. 82A
B2	DM0SAD_H	-	-	-	-	-												W	0000h	Fig. 82B
B4	DM0DAD_L																	W	0000h	Fig. 83A
B6	DM0DAD_H	-	-	-	-	-												W	0000h	Fig. 83B
B8	DM0CNT_L	-	-															W		Fig.84
BA	DM0CNT_H	DMA 0 Control																W/R	0000h	Fig.85
		Enable	Interrupt	Startup Timing		-	Transfer Width	Continuous		Source Address Control		Destination Address Control		-	-	-	-	-		

Fig. 131E

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Fig. in App.
BC	DM1SAD_L	DMA 1 Source Address																W	0000h	Fig. 86A
BE	DM1SAD_H	-	-	-	-	DMA 1 Source Address												W	0000h	Fig. 86B
C0	DM1DAD_L	DMA 1 Destination Address																W	0000h	Fig. 87A
C2	DM1DAD_H	-	-	-	-	-	DMA 1 Destination Address											W	0000h	Fig. 87B
C4	DM1CNT_L	-	-	Word Count														W		Fig. 88
C6	DM1CNT_H	DMA 1 Control: Enable	Interrupt	Startup timing		-	Transfer Width	Contin-uous	Source Address Control		Destination Address Control		-	-	-	-	-	W/R	0000h	Fig. 89
C8	DM2SAD_L	DMA 2 Source Address																W	0000h	Fig. 86A
CA	DM2SAD_H	-	-	-	-	DMA 2 Source Address												W	0000h	Fig. 86B
CC	DM2DAD_L	DMA 2 Destination Address																W	0000h	Fig. 87A
CE	DM2DAD_H	-	-	-	-	-	DMA 2 Destination Address											W	0000h	Fig. 87B
D0	DM2CNT_L	-	-	Word Count														W		Fig. 88
D2	DM2CNT_H	DMA 2 Control: Enable	Interrupt	Startup timing		-	Transfer Width	Contin-uous	Source Address Control		Destination Address Control		-	-	-	-	-	W/R	0000h	Fig. 89
D4	DM3SAD_L	DMA 3 Source Address																W	0000h	Fig. 90A
D6	DM3SAD_H	-	-	-	-	DMA 3 Source Address												W	0000h	Fig. 90B
D8	DM3DAD_L	DMA 3 Destination Address																W	0000h	Fig. 91A
DA	DM3DAD_H	-	-	-	-	DMA 3 Destination Address												W	0000h	Fig. 91B
DC	DM3CNT_L	Word Count																W	0000h	Fig. 92
DE	D3CNT_H	DMA 3 Control: Enable	Interrupt	Startup timing		DREQ	Transfer Width	Contin-uous	Source Address Control		Destination Address Control		-	-	-	-	-	W/R	0000h	Fig. 93

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Fig. in App.
100	TM0D	Timer 0 Setting																W	0000h	Fig. 81A
102	TM0CNT	Timer 0 Control																R/W	0000h	Fig. 81B
		-	-	-	-	-	-	-	-	Operation	Interrupt	-	-	-	Count Up Timing	Prescalar				
104	TM1D	Timer 1 Setting																W	0000h	Fig. 81A
106	TM1CNT	Timer 1 Control																R/W	0000h	Fig. 81B
		-	-	-	-	-	-	-	-	Operation	Interrupt	-	-	-	Count Up Timing	Prescalar				
108	TM2D	Timer 2 Setting																W	0000h	Fig. 81A
10A	TM2CNT	Timer 2 Control																R/W	0000h	Fig. 81B
		-	-	-	-	-	-	-	-	Operation	Interrupt	-	-	-	Count Up Timing	Prescalar				
10C	TM3D	Timer 3 Setting																W	0000h	Fig. 81A
10E	TM3CNT	Timer 3 Control																R/W	0000h	Fig. 81B
		-	-	-	-	-	-	-	-	Operation	Interrupt	-	-	-	Count Up Timing	Prescalar				

Fig. 131F

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Fig. in App.
120	SCD0	32-Bit Normal SIO Communication Data and Multi-play Communication Data 0																R/W	0000h	Fig. 97A
122	SCD1	32-Bit Normal SIO Communication Data and Multi-play Communication Data 1																R/W	0000h	Fig. 97B
124	SCD2	Multi-play Communication Data 2																R/W	0000h	Fig. 104C
126	SCD3	Multi-play Communication Data 3																R/W	0000h	Fig. 104D
128	SCCNT_L	Port Control				SIO Control														
	Normal SIO Communication	-	Interrupt Enable	0	Transfer Bit Length	-	-	-	-	Start	-	-	-	Transfer Enable Flag Send	Transfer Enable Flag Receive	Shift Clock Freq.	Shift Clock	R/W	0000h	Fig. 98
	Multi-play Communication	-	Interrupt Enable	1	0	-	-	-	-	Start (master) Busy (slave)	Communication Error Flag	Multi-play ID		SD Terminal Monitor	SI Terminal Monitor	Baud Rate		R/W	0000h	
	UART Communication	-	Interrupt Enable	1	1	Receive Enable Flag	Send Enable Flag	Parity Enable Flag	FIFO Enable Flag	Data Length	Error Flag	Receive Data Flag	Send Data Flag	Parity Control	CTS Flag	Baud Rate		R/W	0000h	
12A	SCCNT_H	Communication Data																		Fig. 96
	Normal SIO Communication	-	-	-	-	-	-	-	-	8Bit Normal SIO Communication Data								R/W	0000h	
130	P1	-	-	-	-	-	-	L	R	Down	Up	L	R	Start	Select	B	A	R/W	0000h	Fig. 119
132	P1CNT							Key Interrupt												
		Interrupt Conditions	Interrupt Enable	-	-	-	-	L	R	Down	Up	L	R	Start	Select	B	A	R/W	0000h	Fig. 120
134	R	Communication Function Select		-	-	-	-	-	Interrupt Enable	Input/Output Select				Data Bit				R/W	0000h	Fig. 109
										SO	SI	SD	SC	SO	SI	SD	SC			

Fig. 131G

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Fig. in App.
140	HS_CTRL	JOY Bus Communication Control																R/W	0000h	Fig. 110
		-	-	-	-	-	-	-	-	-	Interrupt	-	-	-	Send Complete	Receive Complete	Device reset signal receive			
150	JOYRE_L	JOY Bus Communication Receive Data 0																R/W	0000h	Fig. 111A
152	JOYRE_H	JOY Bus Communication Receive Data 1																R/W	0000h	Fig. 111B
154	JOYTR_L	JOY Bus Communication Send Data 0																R/W	0000h	Fig. 112A
156	JOYTR_H	JOY Bus Communication Send Data 1																R/W	0000h	Fig. 112B
158	JSTAT	JOY Bus Communication Receive Status																R/W	0000h	Fig. 113
		-	-	-	-	-	-	-	-	-	-	General Purpose Flag		Send Status Flag	-	Receive Status Flag	-			
200	IE	Interrupt Enable Flag																R/W	0000h	Fig. 122
		-	-	Game Pak	Key	DMA 3	DMA 2	DMA 1	DMA 0	Entire SIO	TMR3	TMR2	TMR1	TMR0	V Counter Match	H Blank	V Blank			
202	IF	Interrupt Request Flag																R/W	0000h	Fig. 123
		-	-	Game Pak	Key	DMA 3	DMA 2	DMA 1	DMA 0	Entire SIO	TMR3	TMR2	TMR1	TMR0	V Counter Match	H Blank	V Blank			
204	WSCNT	Game Pak Type	Pre-fetch	-	PHI Terminal Output Control		Wait State 2 Wait Control			Wait State 1 Wait Control			Wait State 0 Wait Control			SRAM Wait Control		R/W	0000h	Fig. 17
208	IME	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	Interrupt Master Flag	R/W	0000h	Fig. 121
300	PAUSE	Power Down	Mode	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0000h	

Fig. 131H

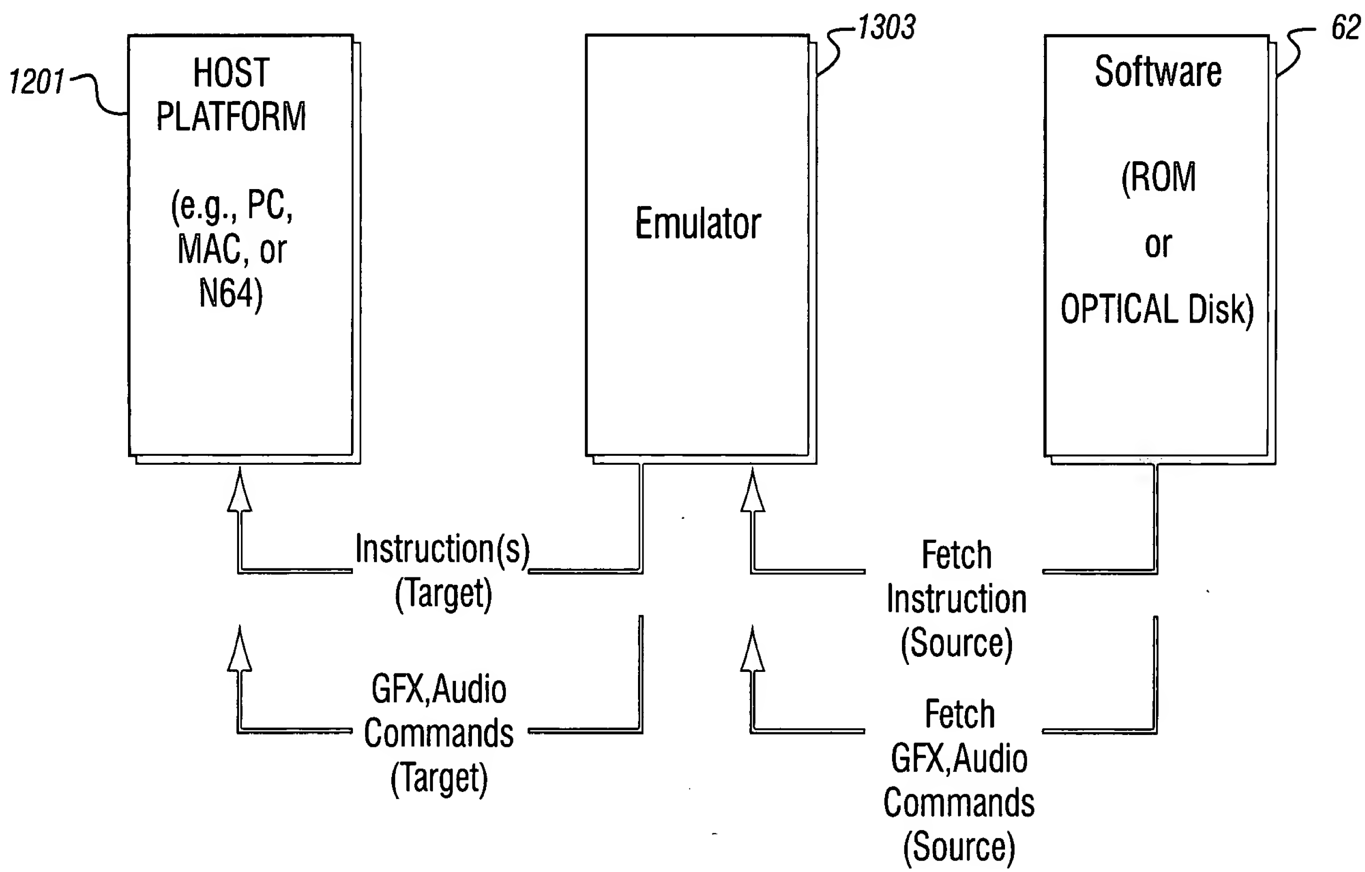


Fig. 132A

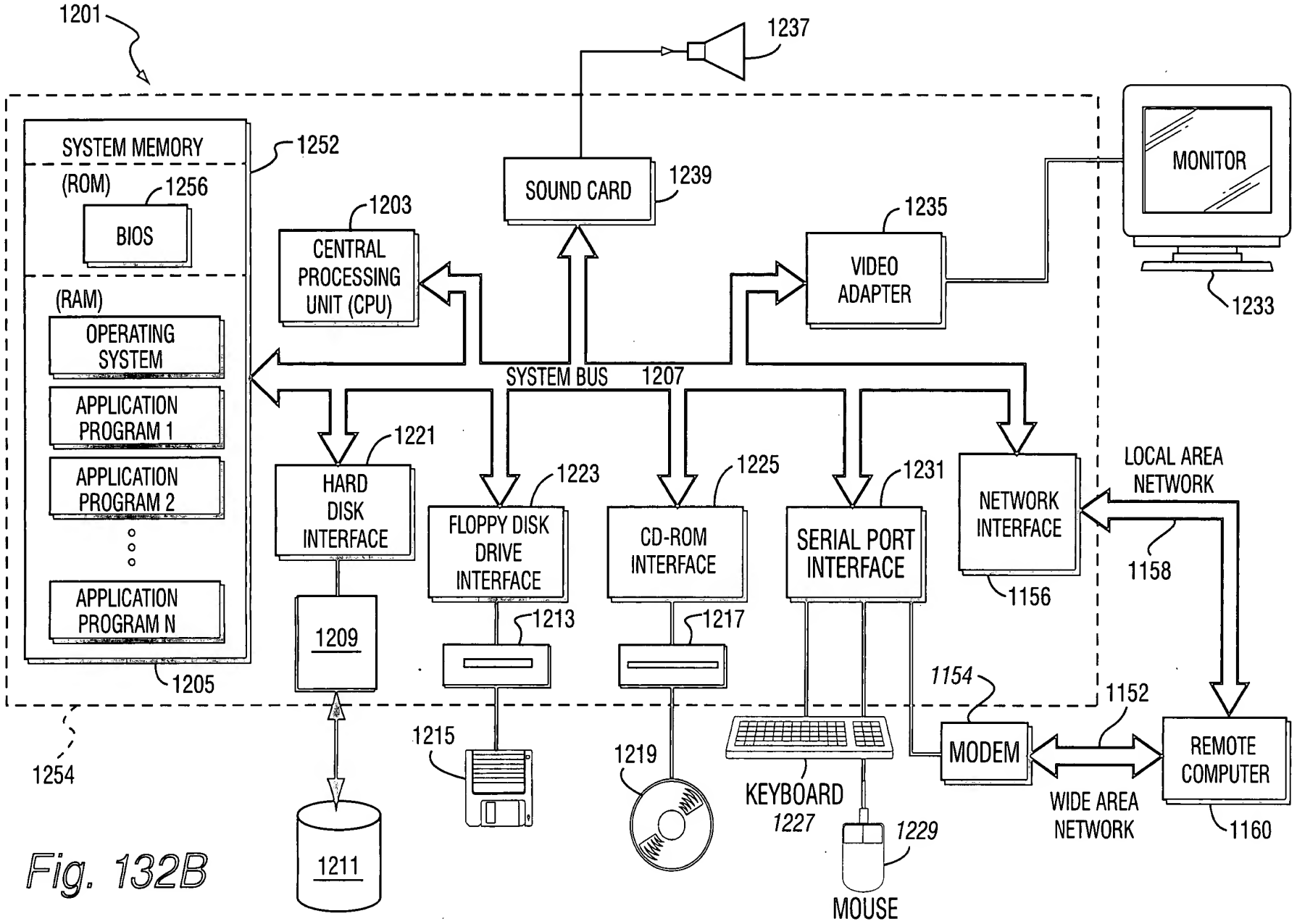

1201
1237
SYSTEM MEMORY
1252
(ROM)
1256
BIOS
(RAM)
OPERATING SYSTEM
APPLICATION PROGRAM 1
APPLICATION PROGRAM 2
APPLICATION PROGRAM N
1205
1254
1203
CENTRAL PROCESSING UNIT (CPU)
SOUND CARD
1239
1235
VIDEO ADAPTER
MONITOR
1233
SYSTEM BUS
1207
1221
HARD DISK INTERFACE
1209
1211
1223
FLOPPY DISK DRIVE INTERFACE
1213
1215
1225
CD-ROM INTERFACE
1217
1219
1231
SERIAL PORT INTERFACE
KEYBOARD
1227
MOUSE
1229
NETWORK INTERFACE
1156
LOCAL AREA NETWORK
1158
1154
MODEM
1152
WIDE AREA NETWORK
REMOTE COMPUTER
1160

Fig. 132B

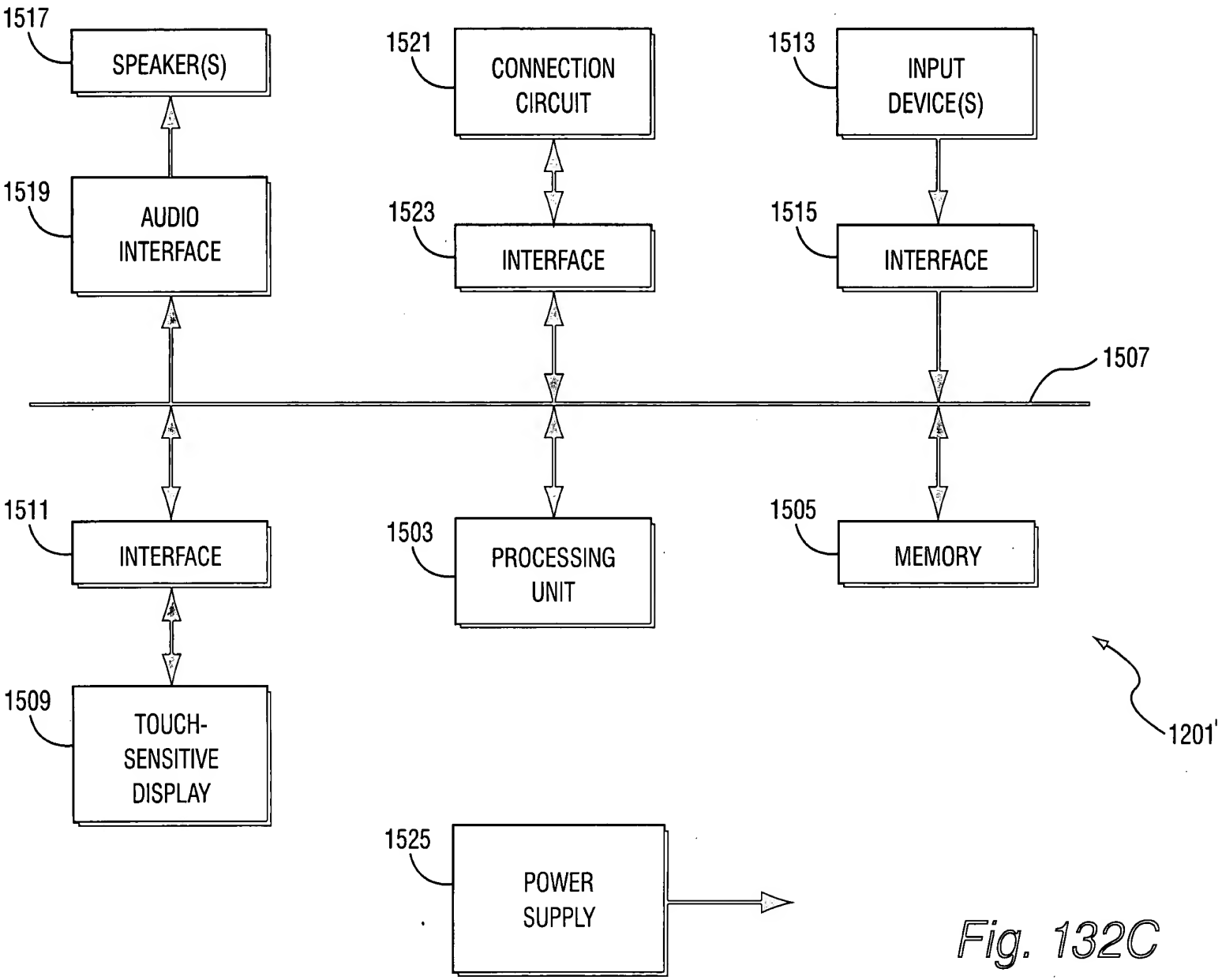
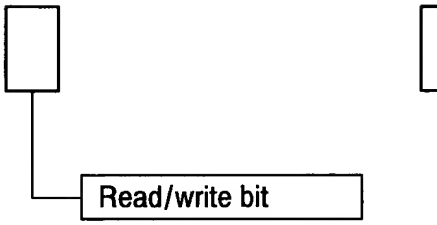
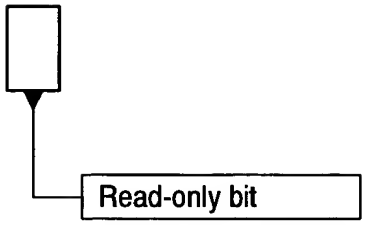

1517
SPEAKER(S)
1521
CONNECTION CIRCUIT
1513
INPUT DEVICE(S)
1519
AUDIO INTERFACE
1523
INTERFACE
1515
INTERFACE
1507
1511
INTERFACE
1503
PROCESSING UNIT
1505
MEMORY
1509
TOUCH-SENSITIVE DISPLAY
1201'
1525
POWER SUPPLY

Fig. 132C



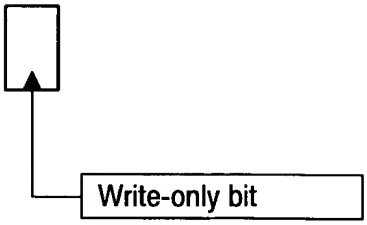
A readable and writable bit.

Fig. 133A



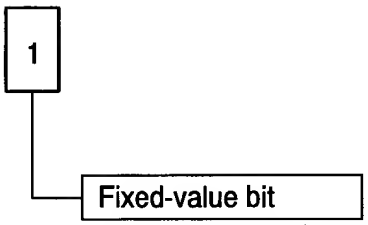
A bit that is readable but not writable.

Fig. 133B



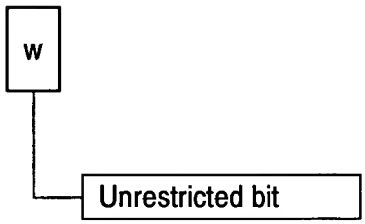
A bit that is not readable but is writable.

Fig. 133C



Must be set to a specified fixed value.

Fig. 133D



Can be set to either 0 or 1.

Fig. 133E

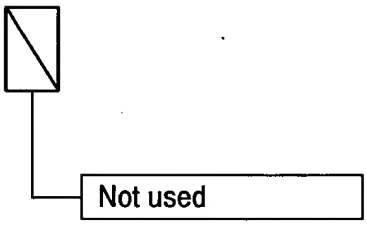


Fig. 133F